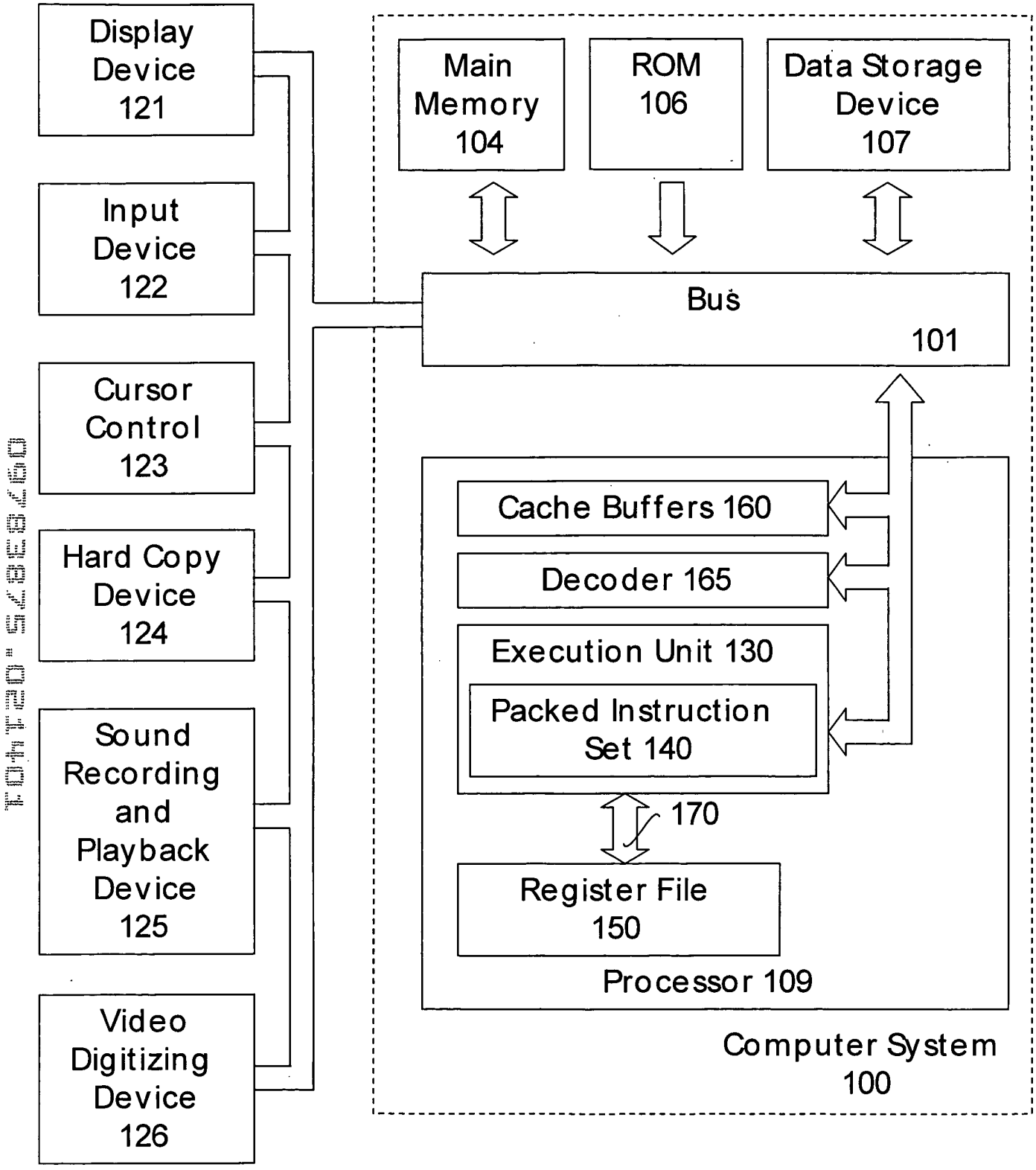

Display Device 121
Input Device 122
Cursor Control 123
Hard Copy Device 124
Sound Recording and Playback Device 125
Video Digitizing Device 126
Main Memory 104
ROM 106
Data Storage Device 107
Bus 101
Cache Buffers 160
Decoder 165
Execution Unit 130
Packed Instruction Set 140
170
Register File 150
Processor 109
Computer System 100

FIG. 1

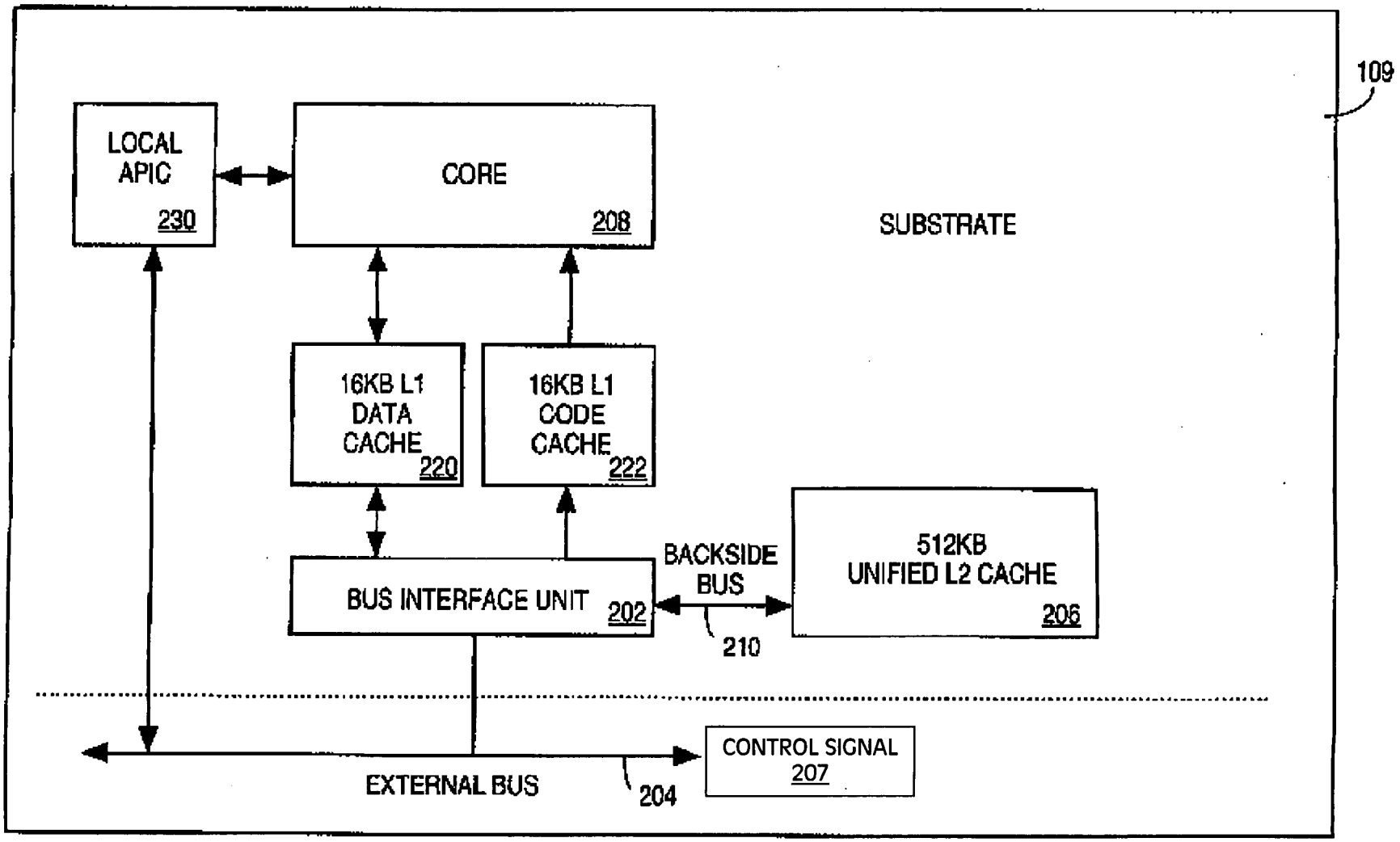


Fig. 2

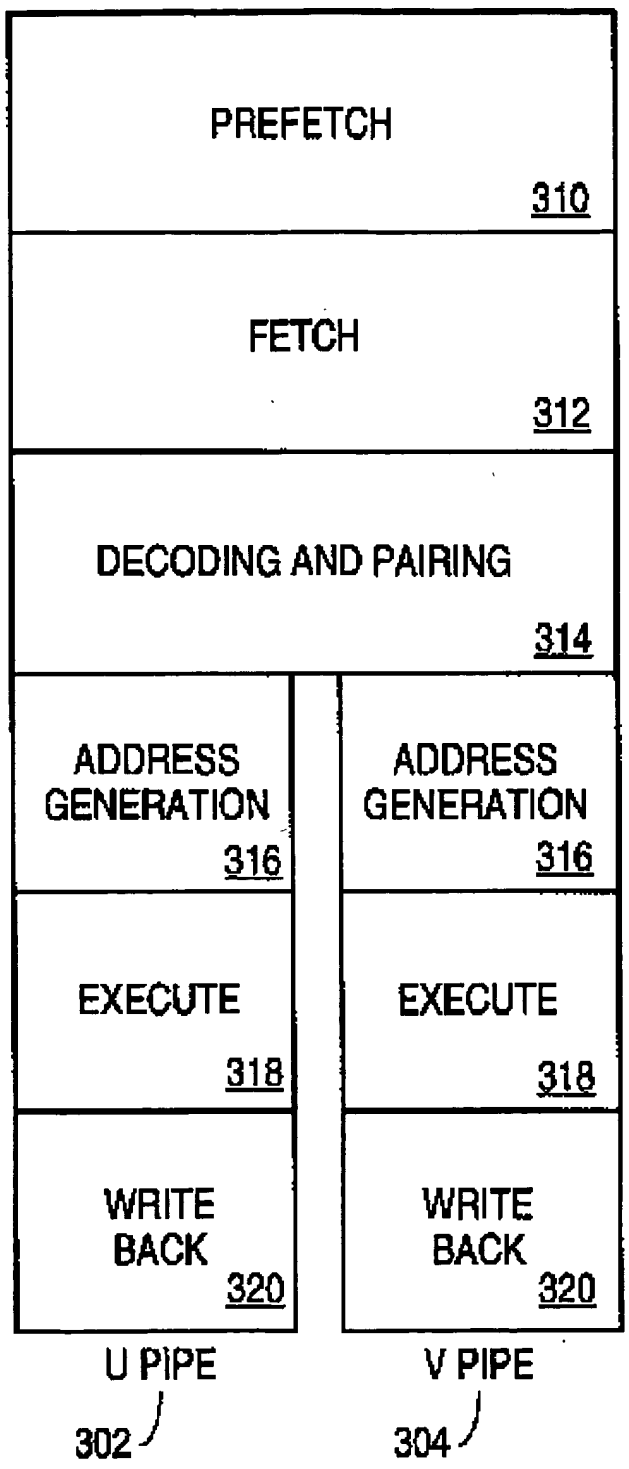

300
PREFETCH
310
FETCH
312
DECODING AND PAIRING
314
ADDRESS GENERATION
316
ADDRESS GENERATION
316
EXECUTE
318
EXECUTE
318
WRITE BACK
320
WRITE BACK
320
U PIPE
302
V PIPE
304

Fig. 3

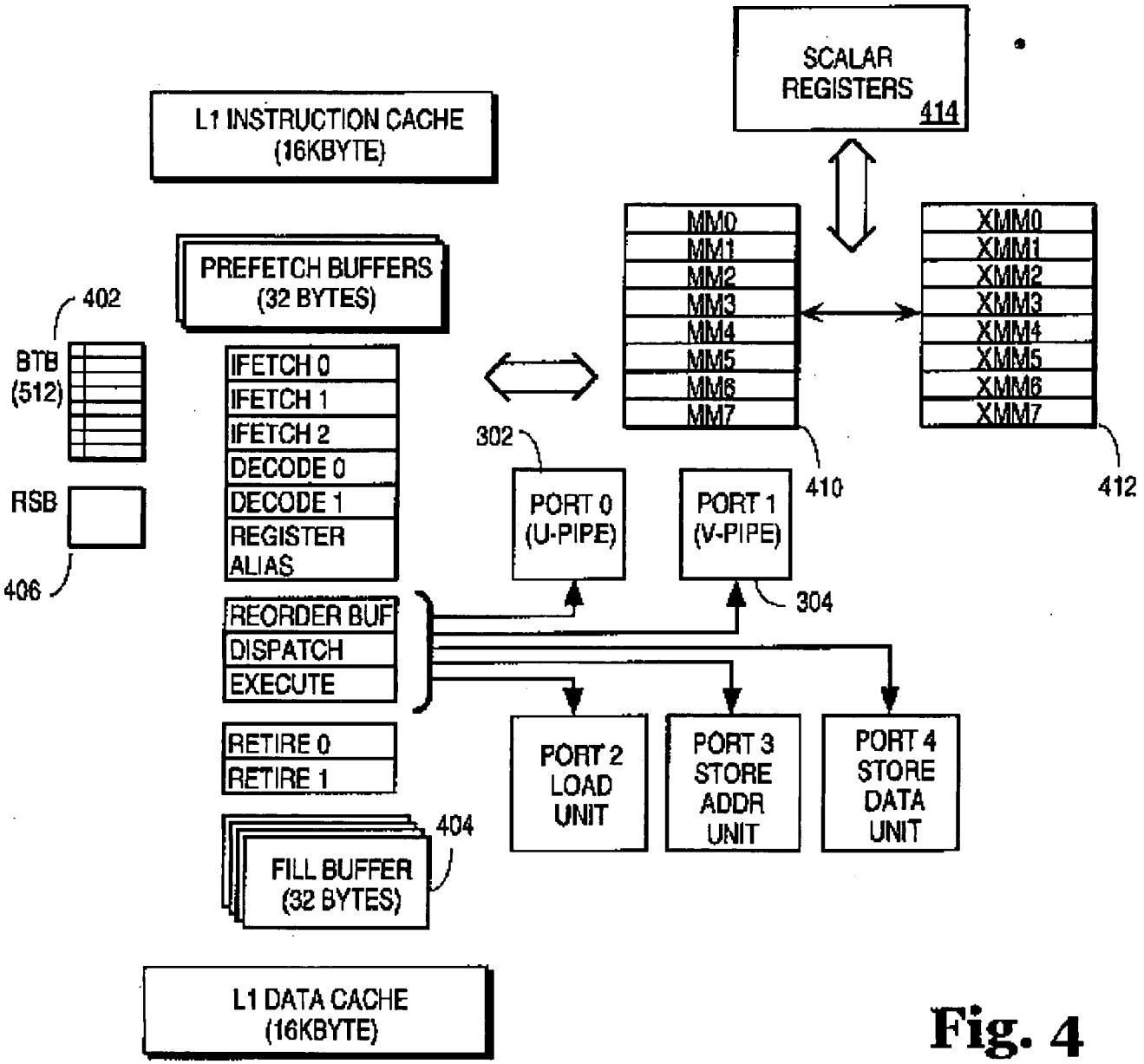


Fig. 4

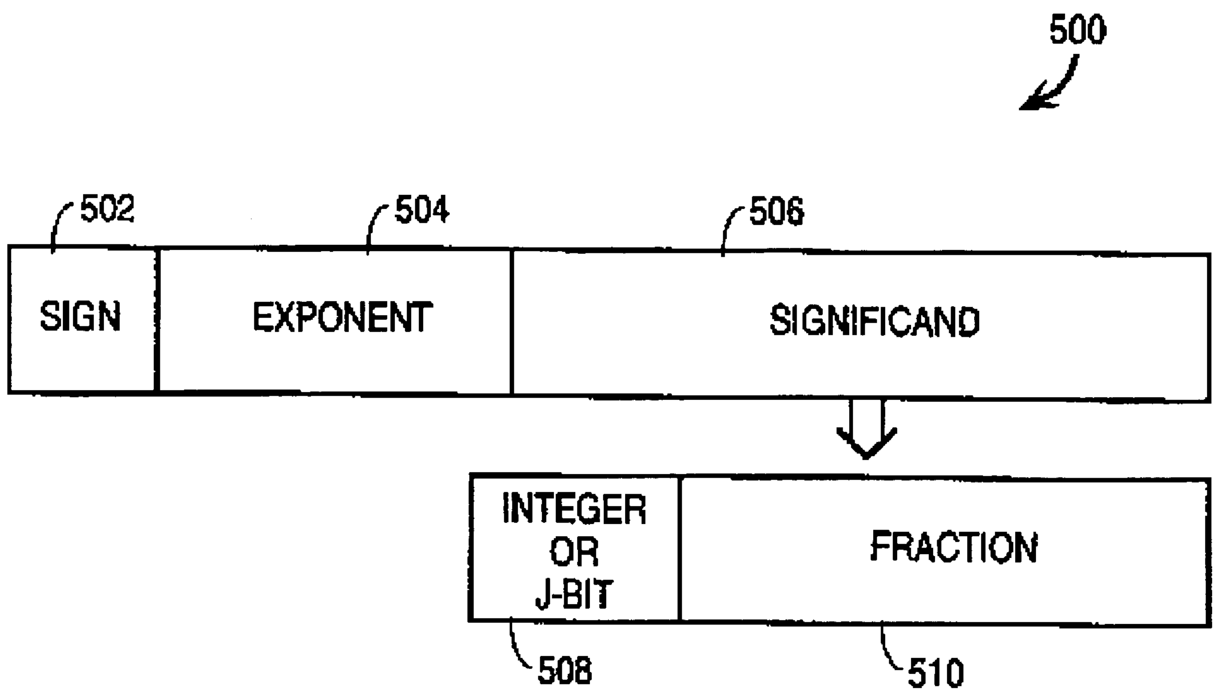

500
502
504
506
SIGN
EXPONENT
SIGNIFICAND
INTEGER OR J-BIT
FRACTION
508
510

FIG. 5a

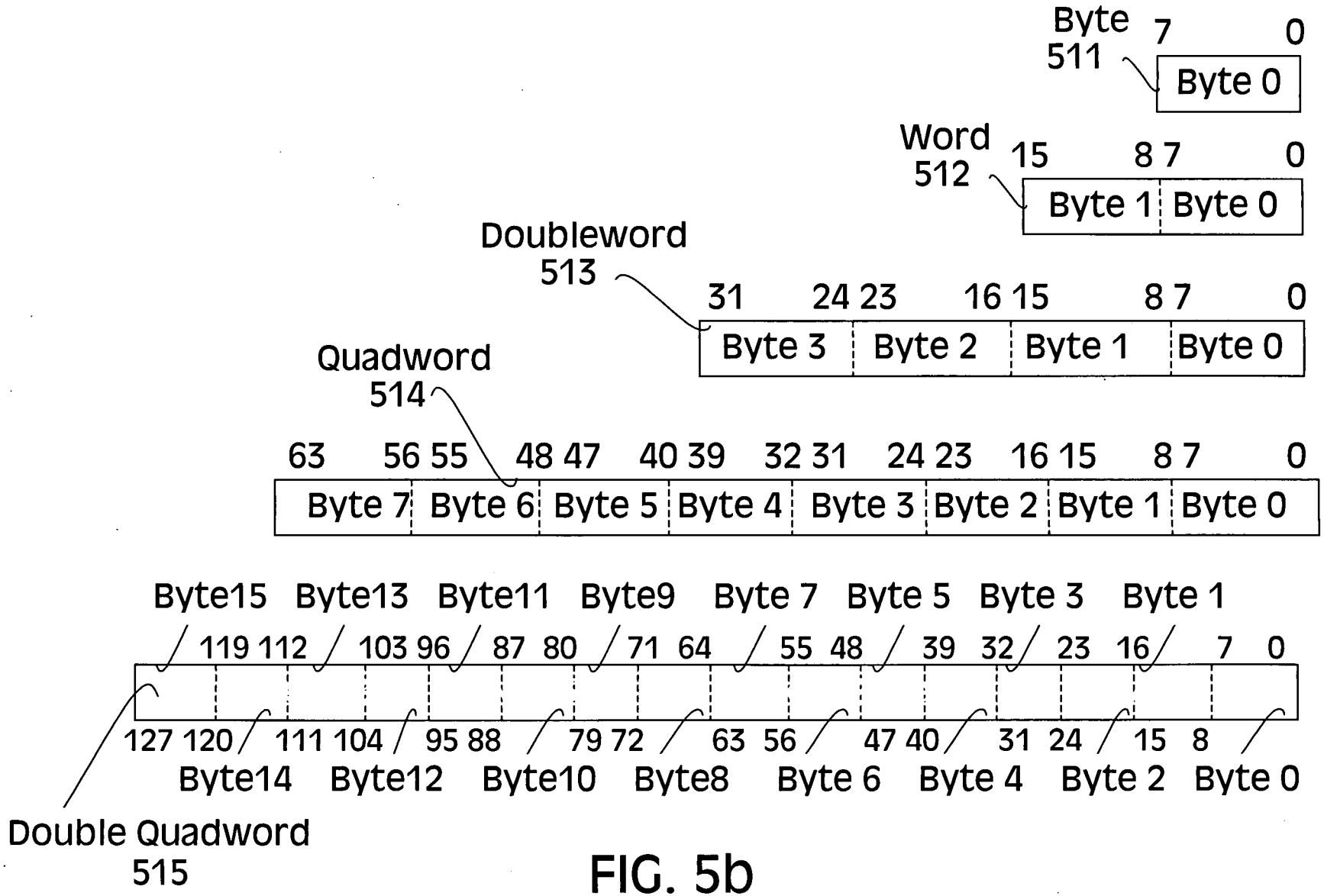
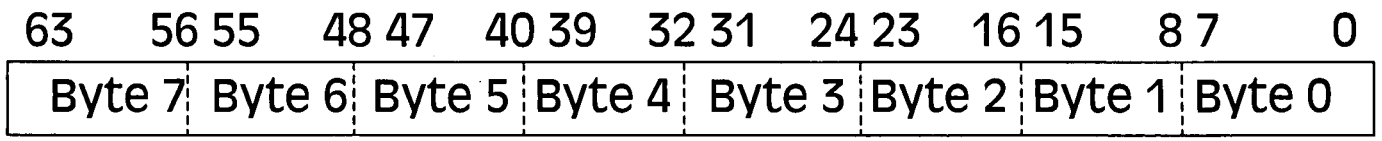
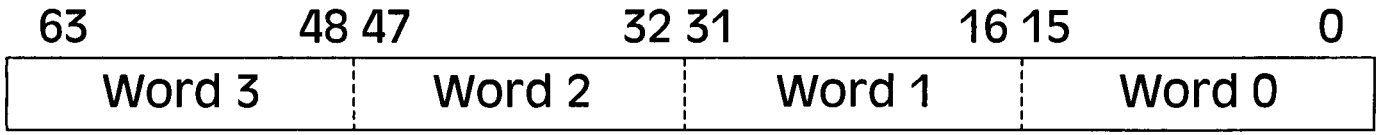


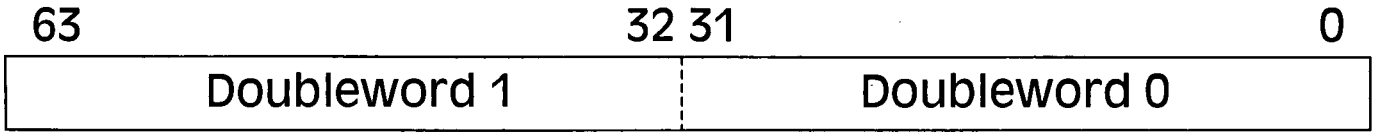
FIG. 5b



Packed Byte 521

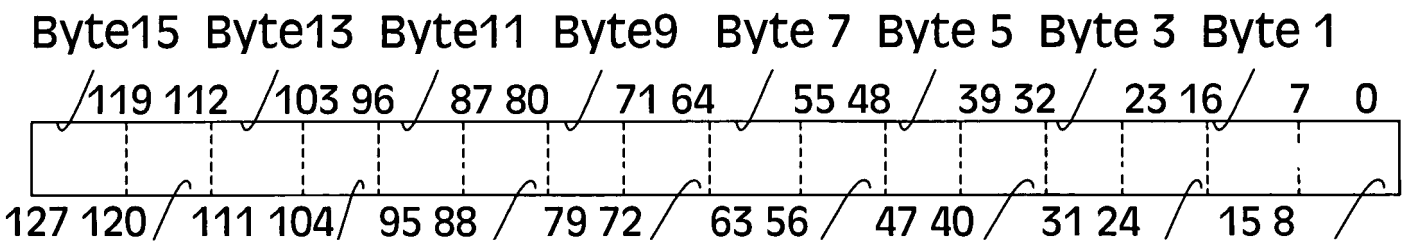


Packed Word 522

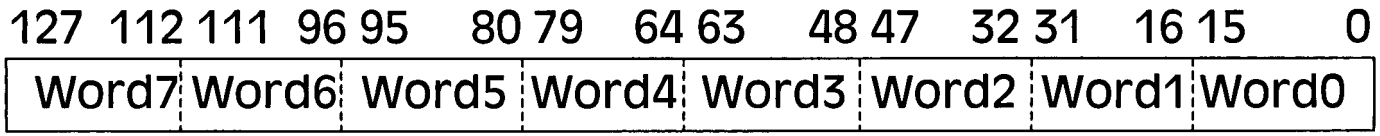


Packed Doubleword 523

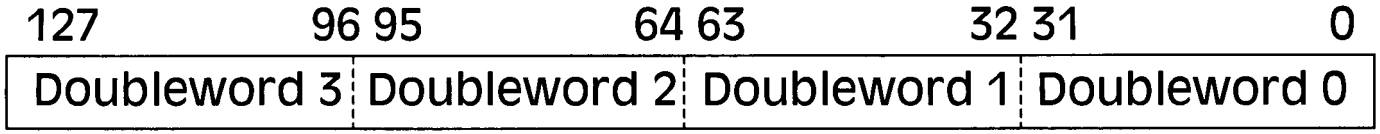
FIG. 5C



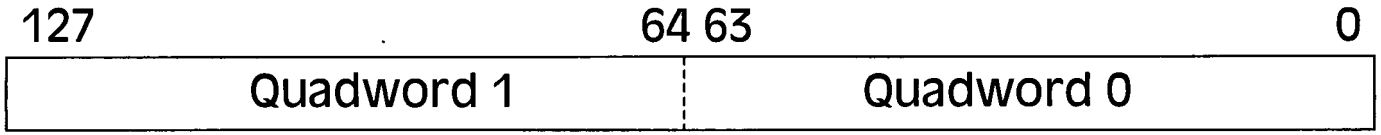
Packed Byte 524



Packed Word 525



Packed Doubleword 526



Packed Quadword 527

FIG. 5d

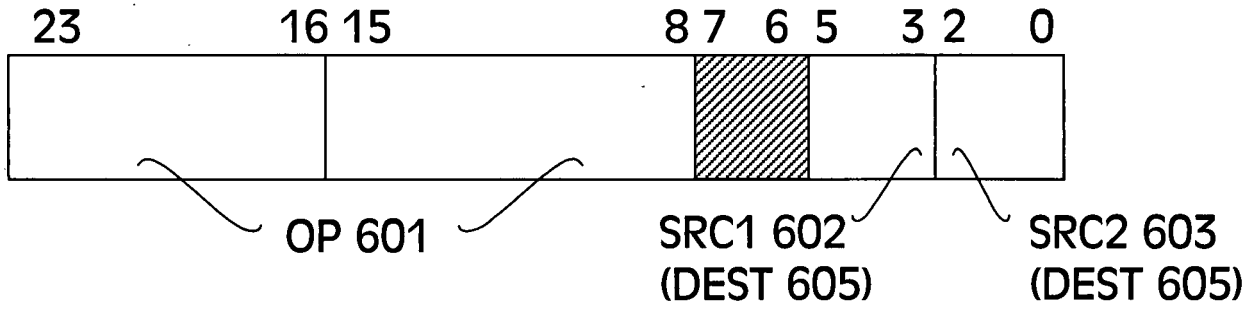


FIG. 6a

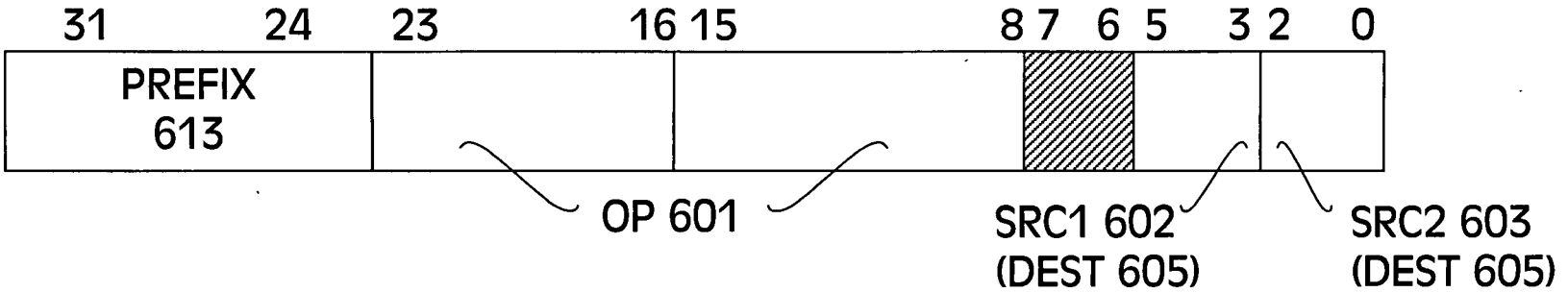


FIG. 6b

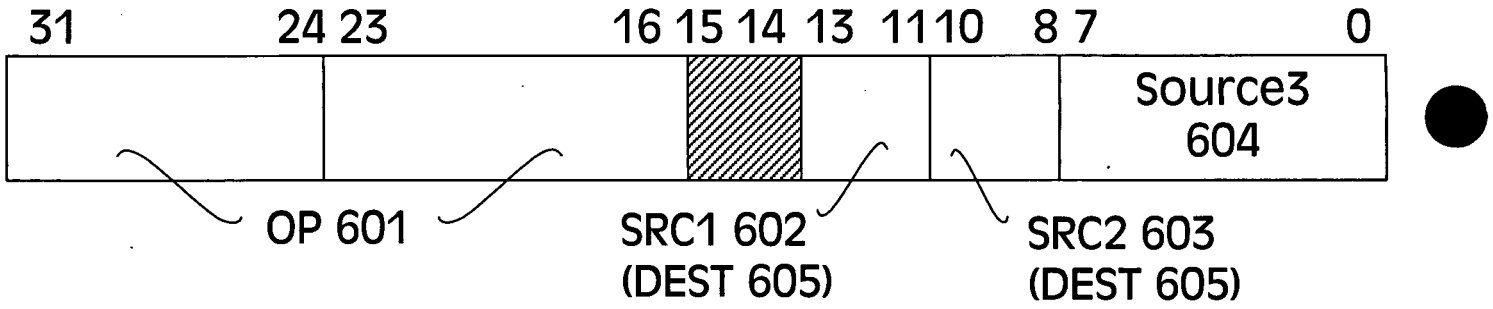


FIG. 6c

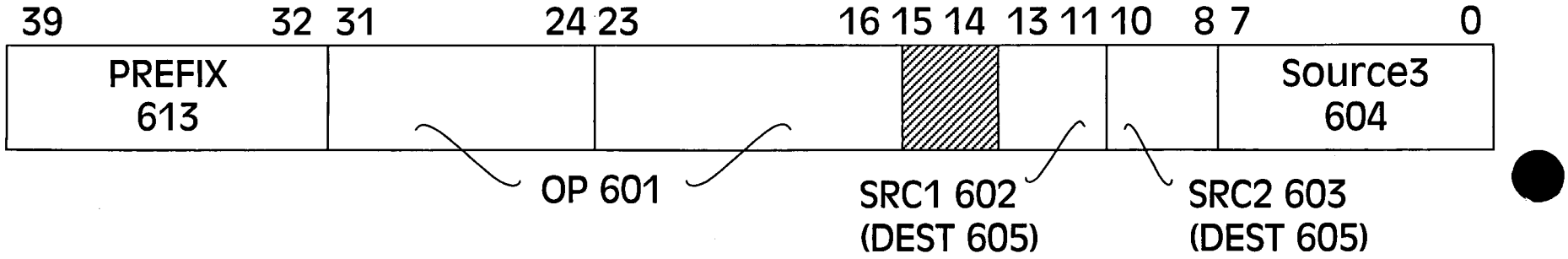


FIG. 6d

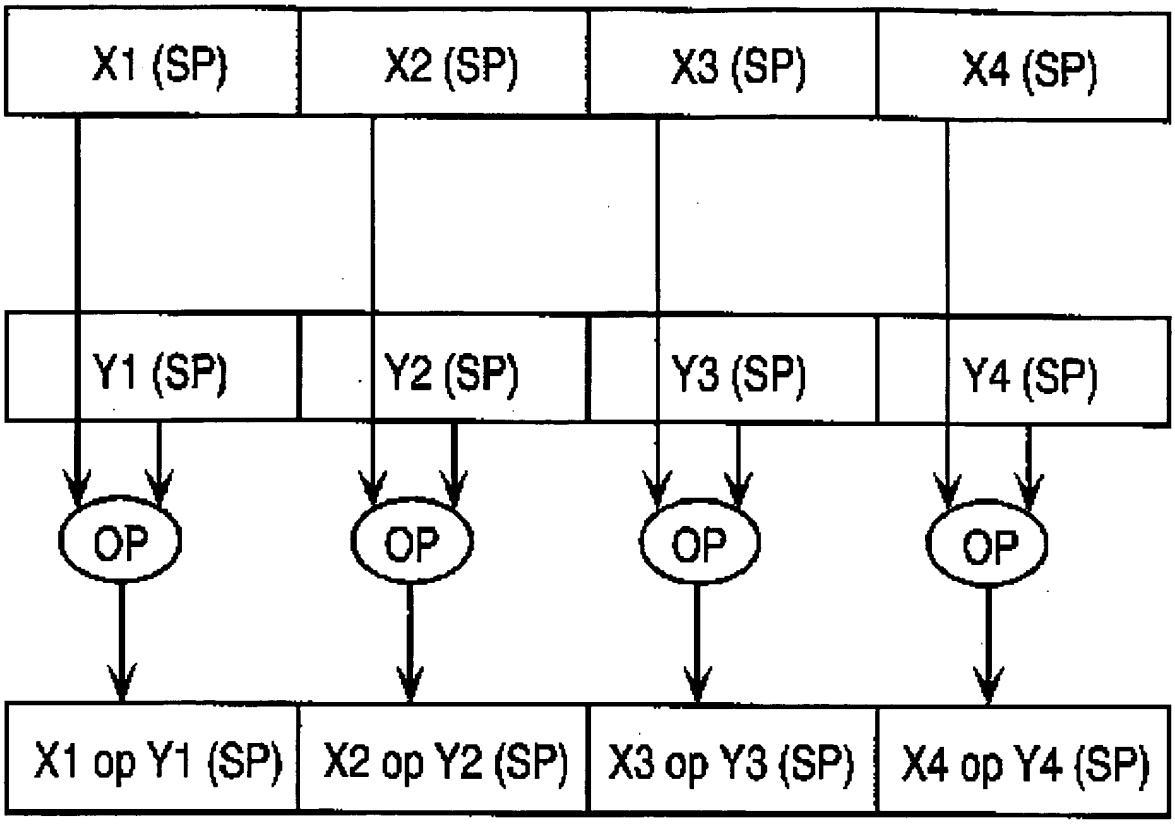


FIG. 7a

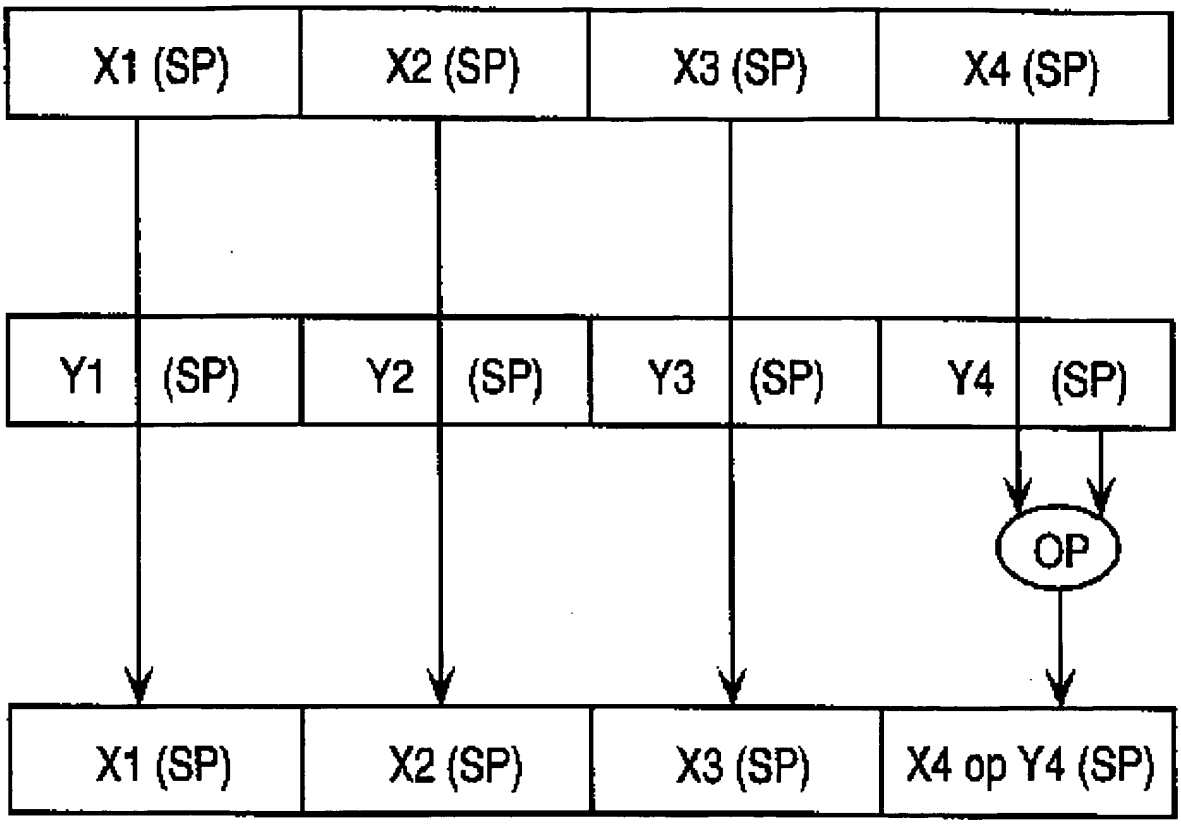

X1 (SP)
X2 (SP)
X3 (SP)
X4 (SP)
Y1
(SP)
Y2
(SP)
Y3
(SP)
Y4
(SP)
OP
X1 (SP)
X2 (SP)
X3 (SP)
X4 op Y4 (SP)

FIG. 7b

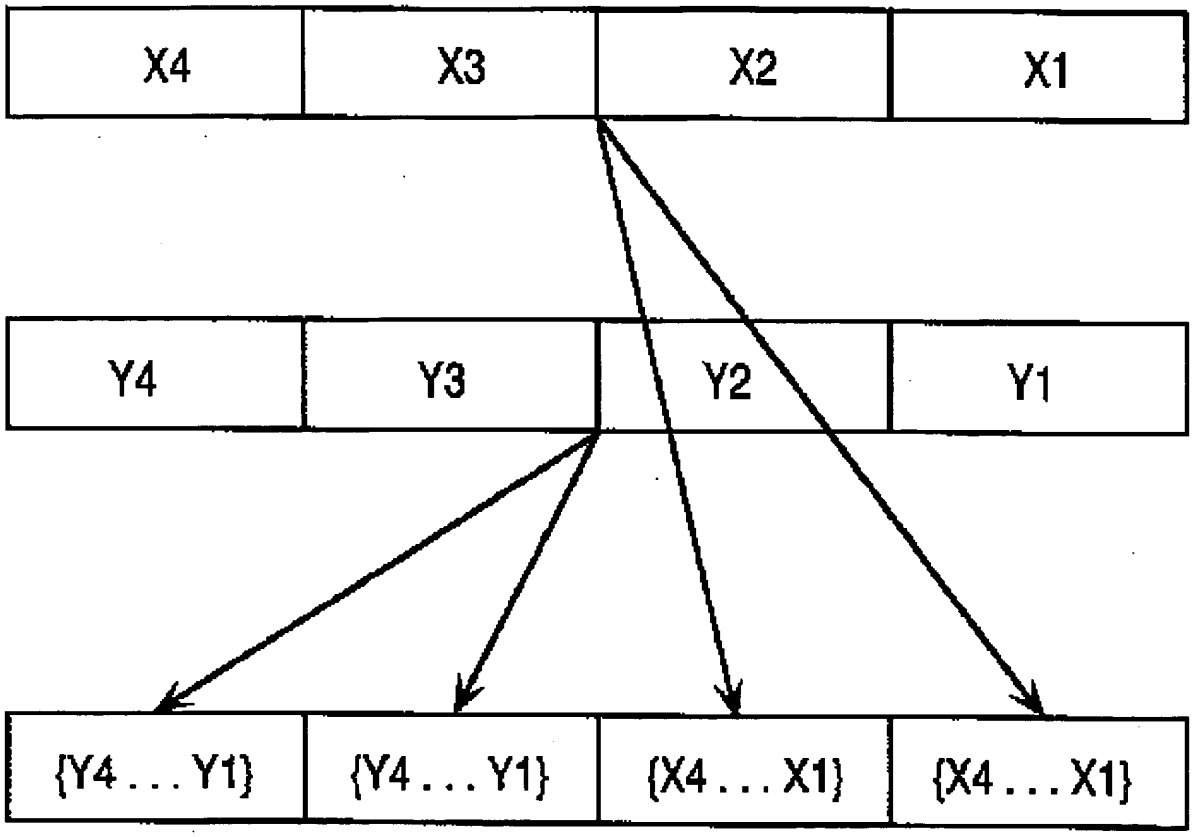


Fig. 8

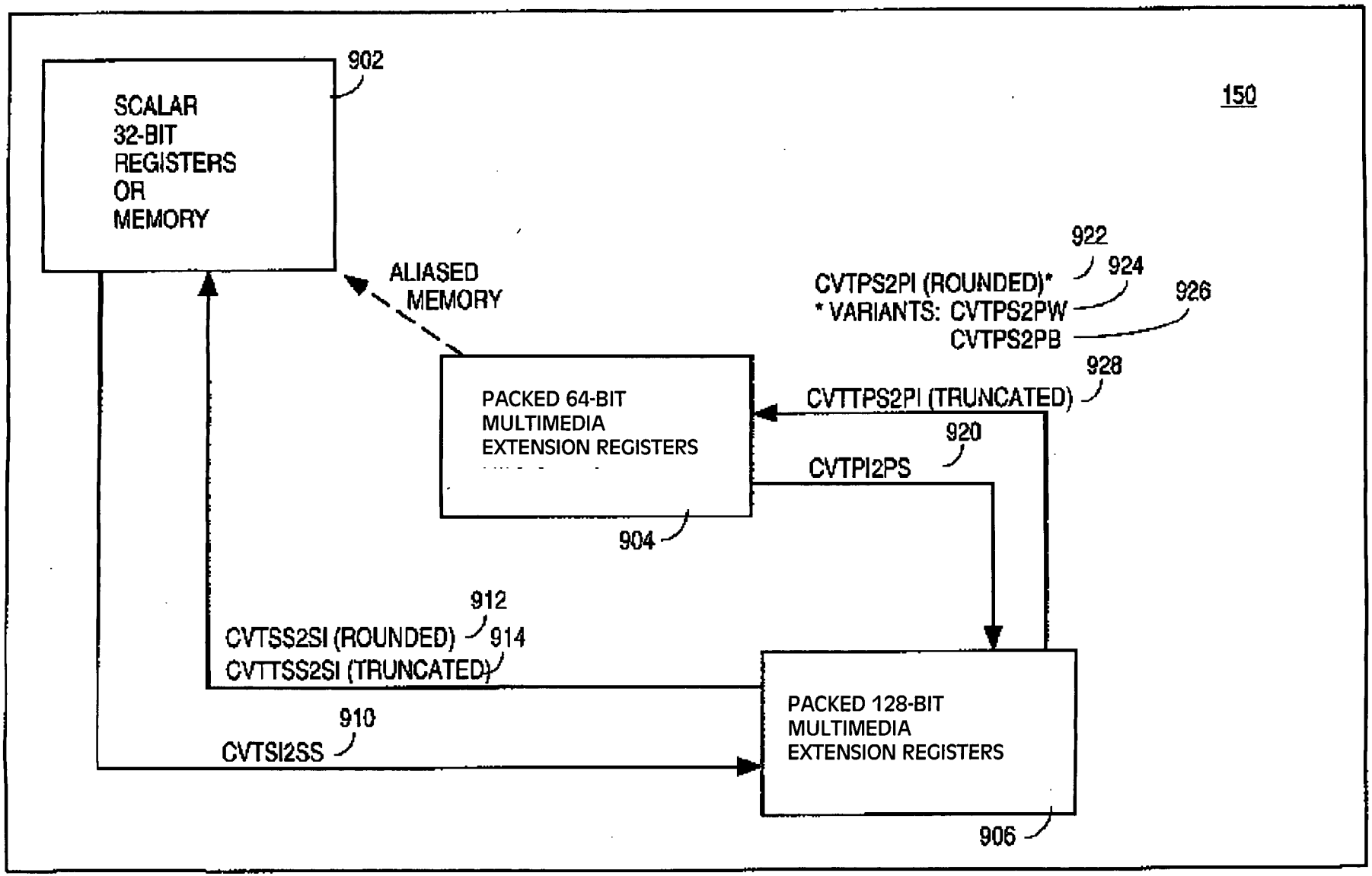

902
SCALAR
32-BIT
REGISTERS
OR
MEMORY
150
ALIASED
MEMORY
922
924
CVTPS2PI (ROUNDED)*
* VARIANTS: CVTPS2PW
926
CVTPS2PB
928
CVTTPS2PI (TRUNCATED)
PACKED 64-BIT
MULTIMEDIA
EXTENSION REGISTERS
920
CVTPI2PS
904
912
CVTSS2SI (ROUNDED)
914
CVTTSS2SI (TRUNCATED)
910
CVTSI2SS
PACKED 128-BIT
MULTIMEDIA
EXTENSION REGISTERS
906

FIG. 9a

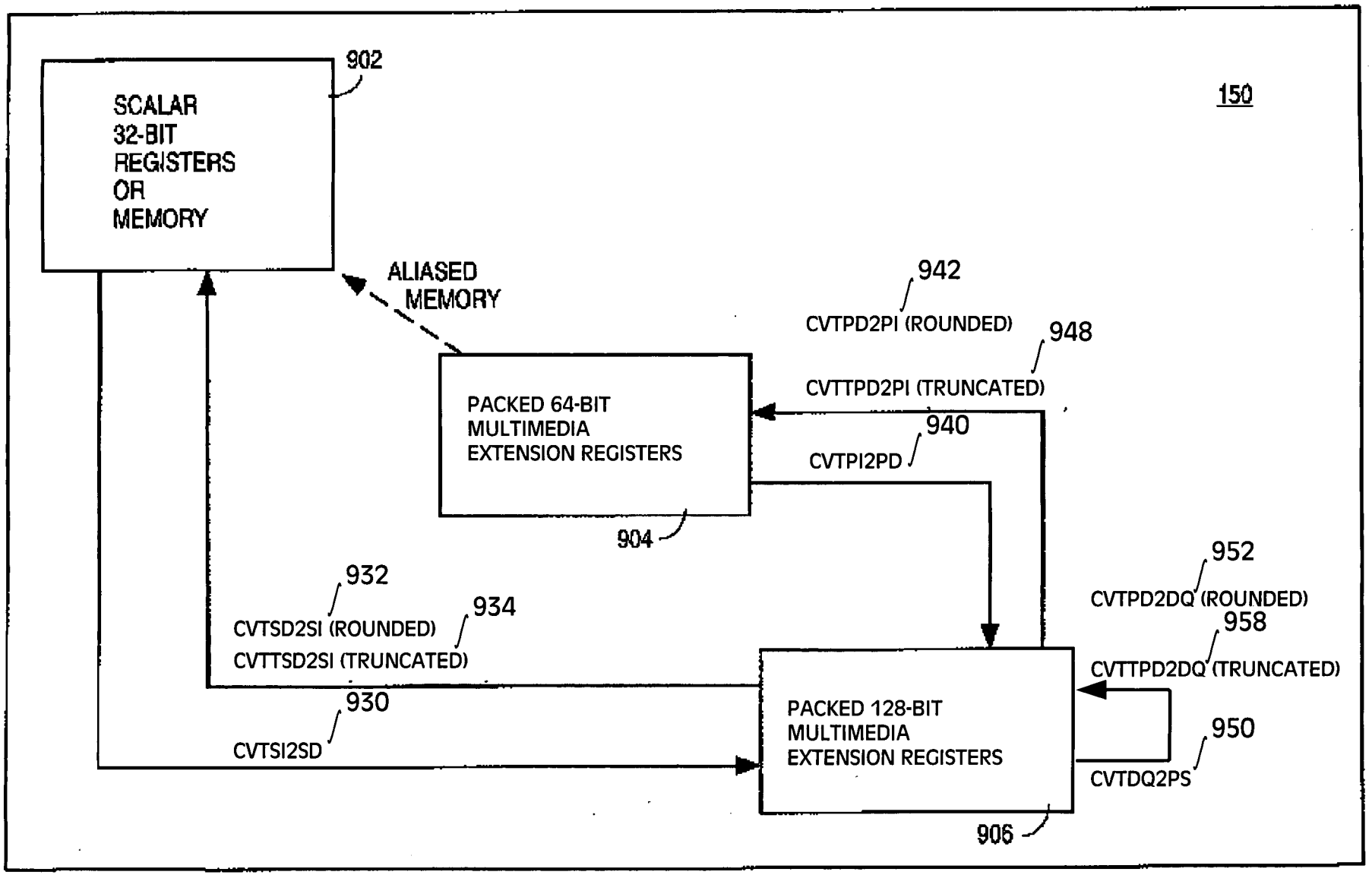
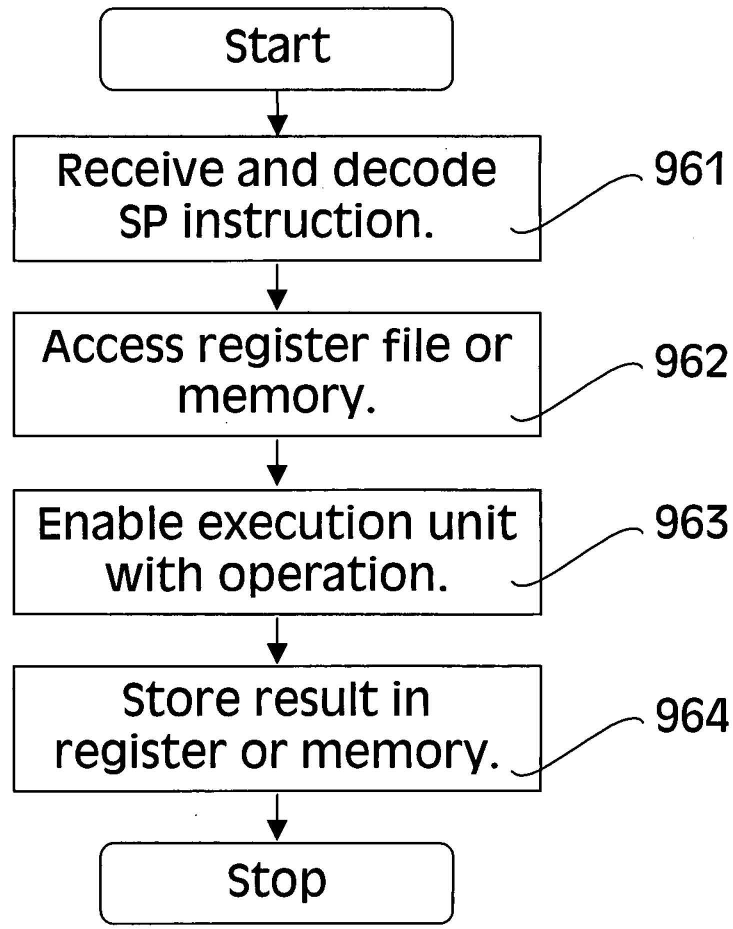

902
SCALAR
32-BIT
REGISTERS
OR
MEMORY
150
ALIASED
MEMORY
942
CVTPD2PI (ROUNDED)
948
CVTTPD2PI (TRUNCATED)
PACKED 64-BIT
MULTIMEDIA
EXTENSION REGISTERS
940
CVTPI2PD
904
952
CVTPD2DQ (ROUNDED)
958
CVTTPD2DQ (TRUNCATED)
932
CVTSD2SI (ROUNDED)
934
CVTTSD2SI (TRUNCATED)
930
CVTSI2SD
PACKED 128-BIT
MULTIMEDIA
EXTENSION REGISTERS
950
CVTDQ2PS
906

FIG. 9b

FIG. 9c



Start
Receive and decode SP instruction.
961
Access register file or memory.
962
Enable execution unit with operation.
963
Store result in register or memory.
964
Stop

FIG. 9d

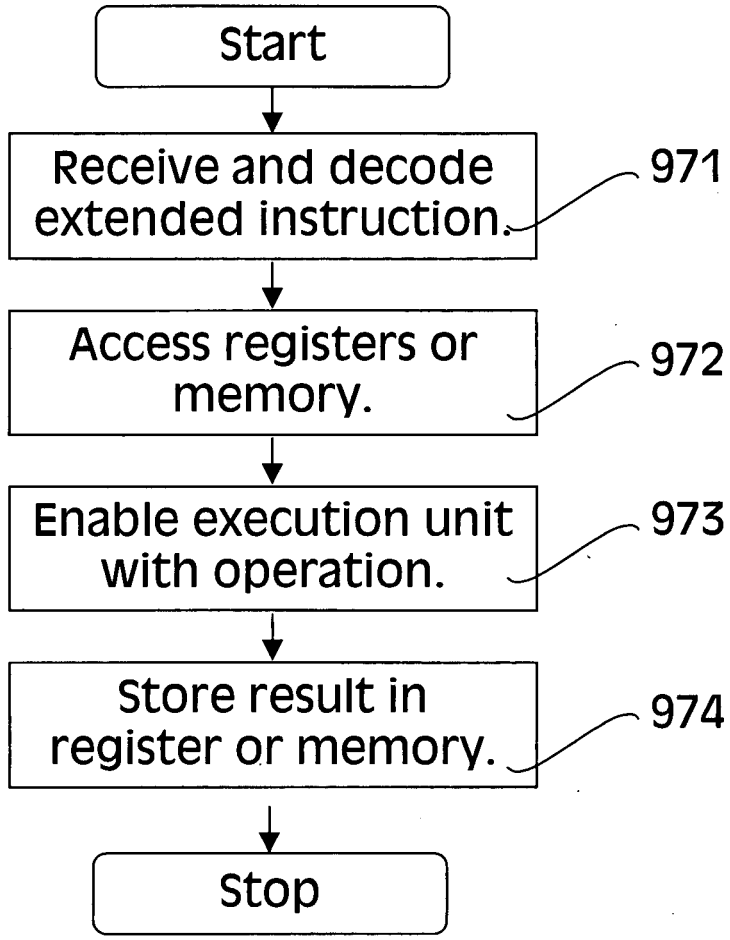
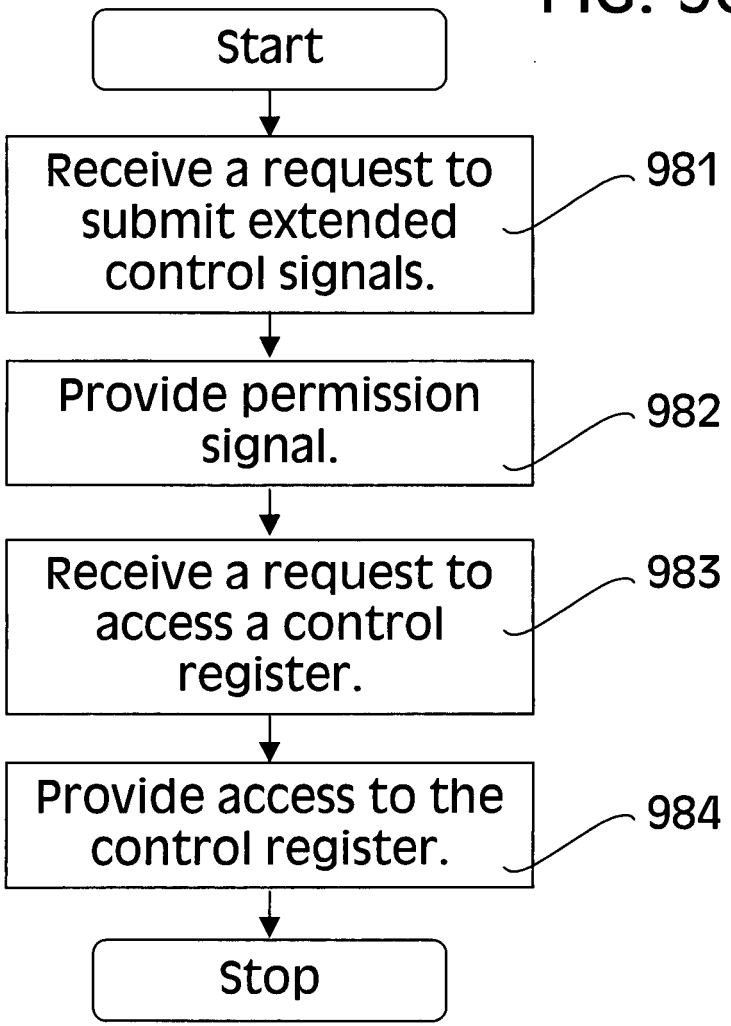


FIG. 9e


Start
Receive a request to submit extended control signals.
981
Provide permission signal.
982
Receive a request to access a control register.
983
Provide access to the control register.
984
Stop

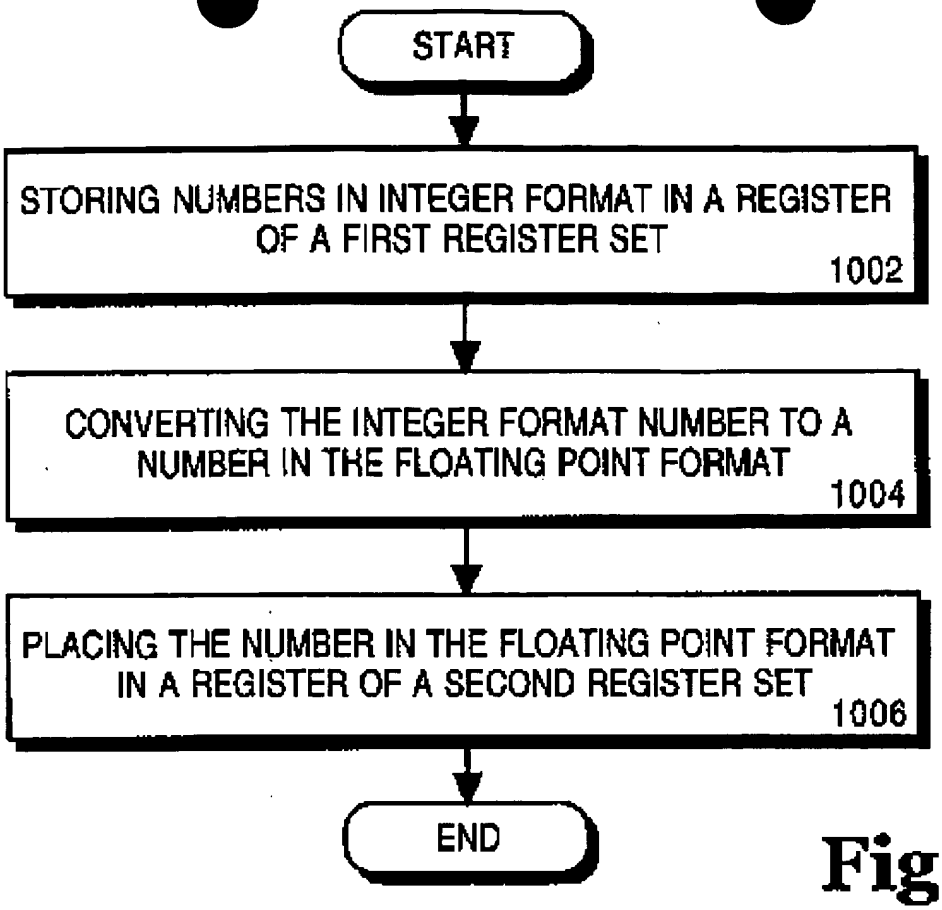


Fig. 10

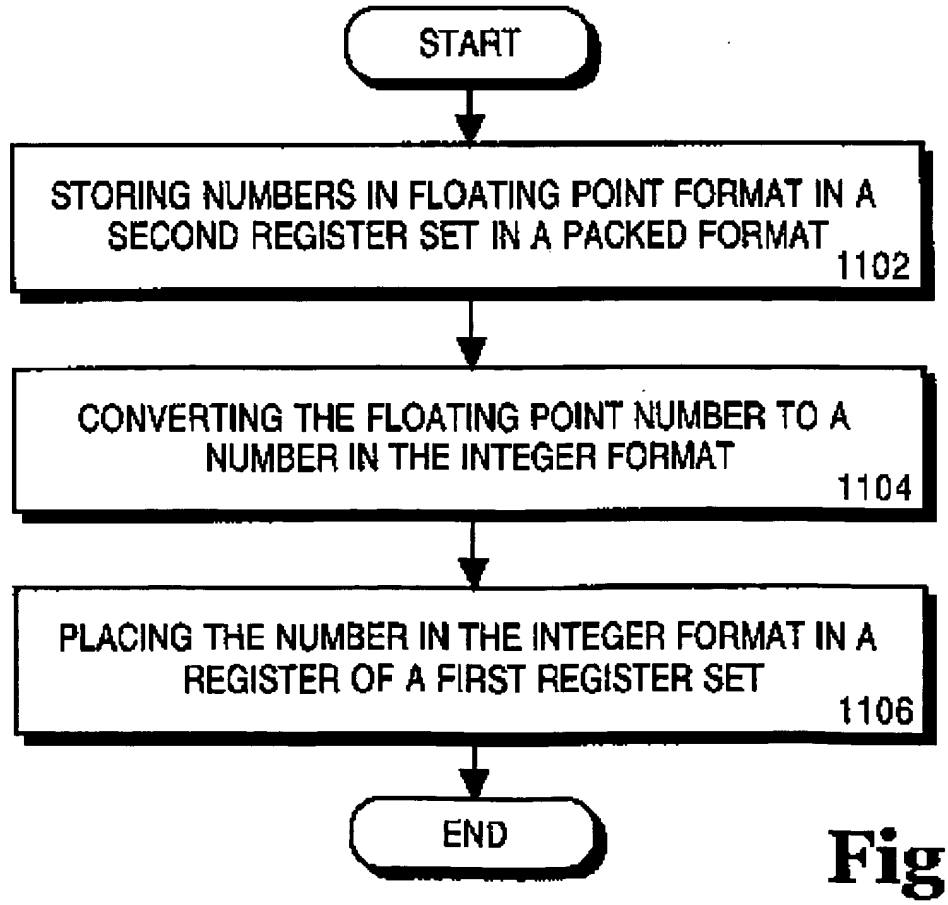


Fig. 11

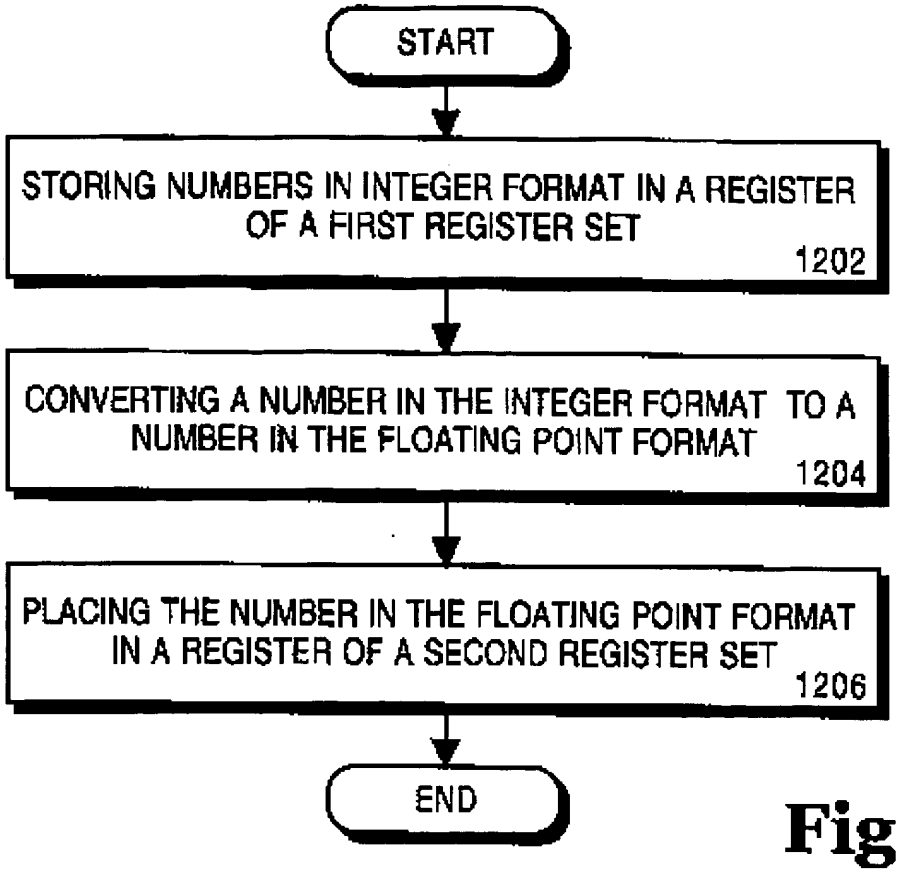

START
STORING NUMBERS IN INTEGER FORMAT IN A REGISTER OF A FIRST REGISTER SET
1202
CONVERTING A NUMBER IN THE INTEGER FORMAT TO A NUMBER IN THE FLOATING POINT FORMAT
1204
PLACING THE NUMBER IN THE FLOATING POINT FORMAT IN A REGISTER OF A SECOND REGISTER SET
1206
END

Fig. 12

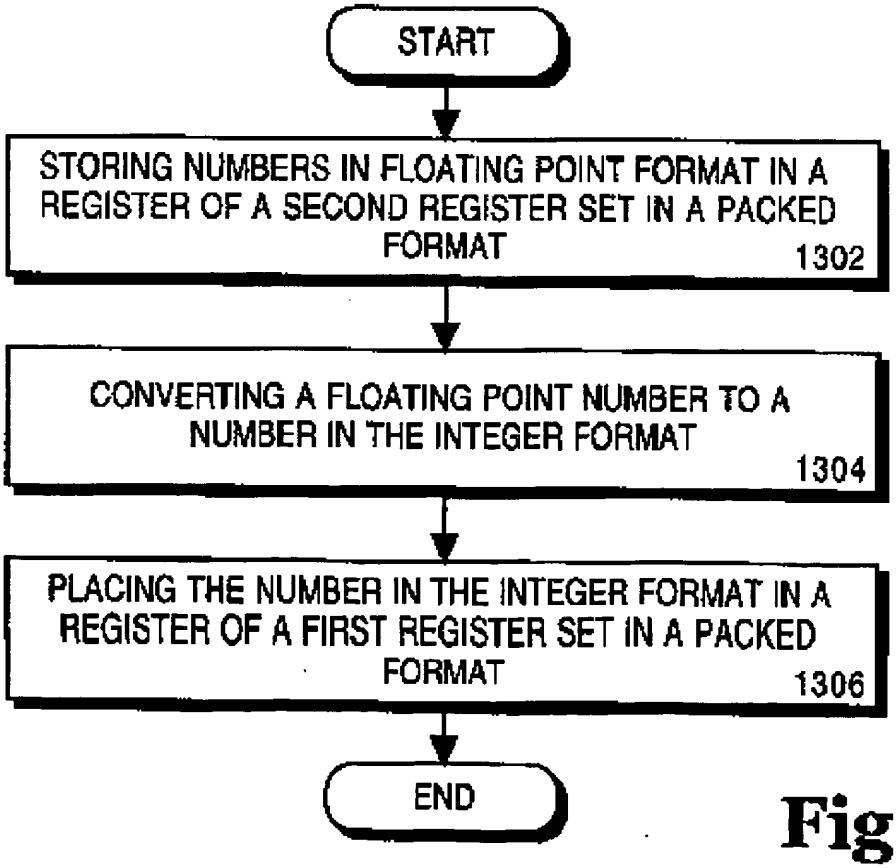

START
STORING NUMBERS IN FLOATING POINT FORMAT IN A REGISTER OF A SECOND REGISTER SET IN A PACKED FORMAT
1302
CONVERTING A FLOATING POINT NUMBER TO A NUMBER IN THE INTEGER FORMAT
1304
PLACING THE NUMBER IN THE INTEGER FORMAT IN A REGISTER OF A FIRST REGISTER SET IN A PACKED FORMAT
1306
END

Fig. 13

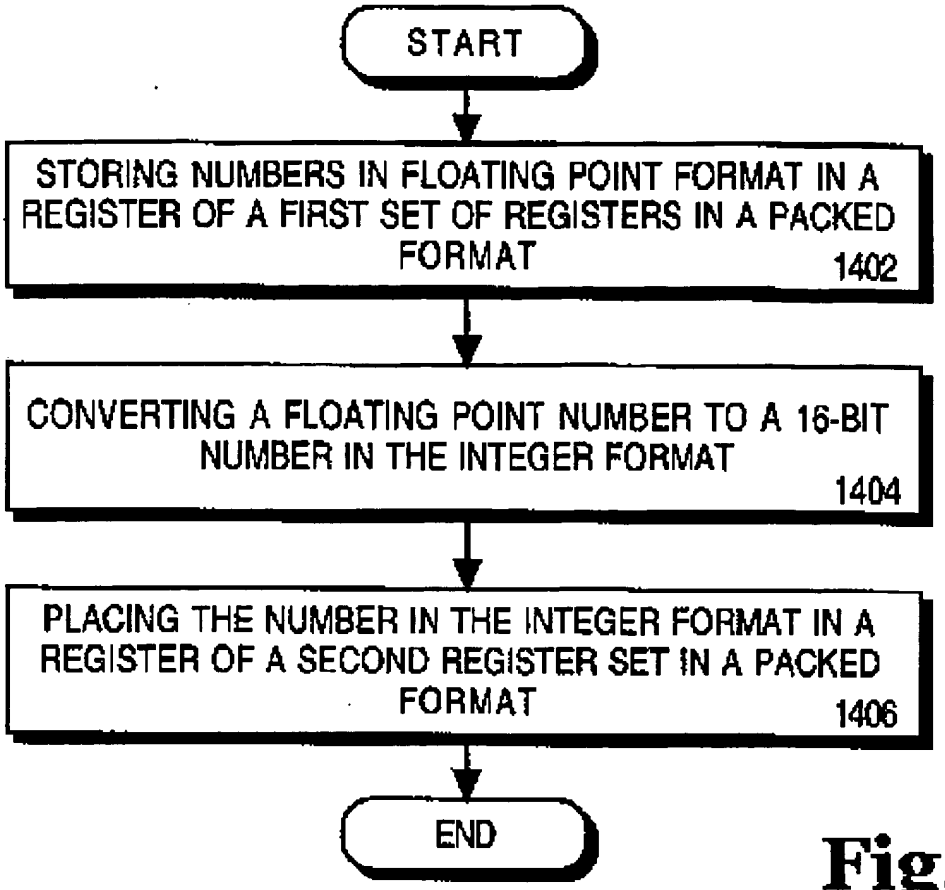

START
STORING NUMBERS IN FLOATING POINT FORMAT IN A REGISTER OF A FIRST SET OF REGISTERS IN A PACKED FORMAT
1402
CONVERTING A FLOATING POINT NUMBER TO A 16-BIT NUMBER IN THE INTEGER FORMAT
1404
PLACING THE NUMBER IN THE INTEGER FORMAT IN A REGISTER OF A SECOND REGISTER SET IN A PACKED FORMAT
1406
END

Fig. 14

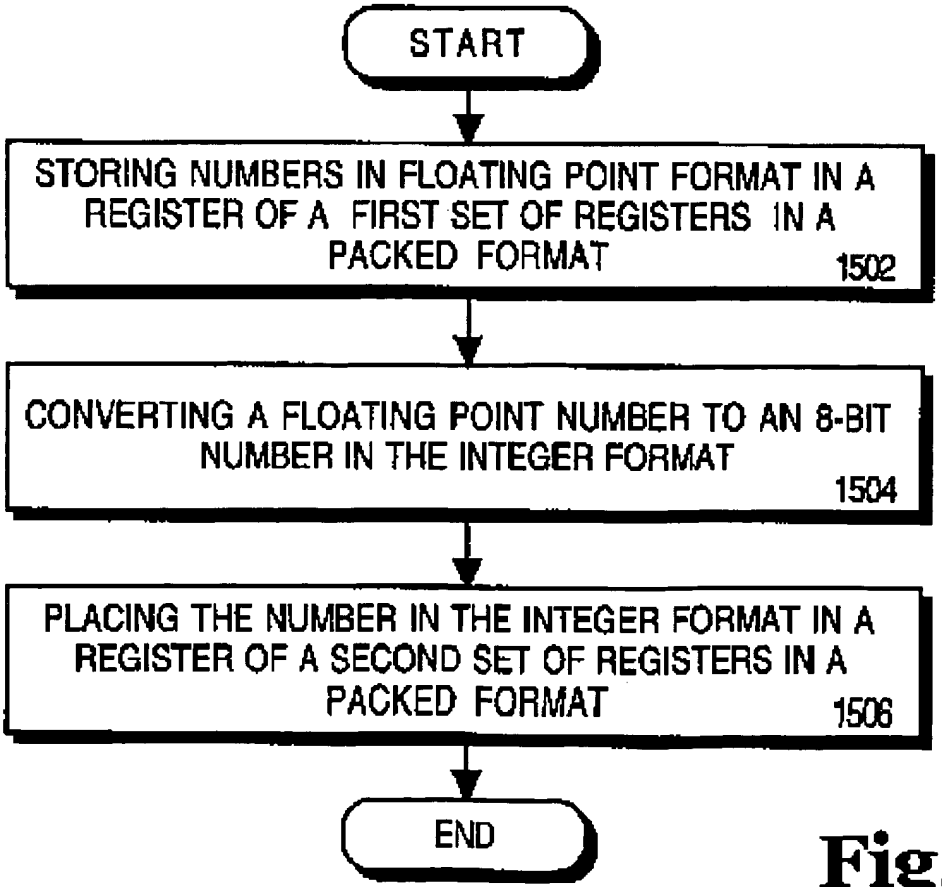

START
STORING NUMBERS IN FLOATING POINT FORMAT IN A REGISTER OF A FIRST SET OF REGISTERS IN A PACKED FORMAT
1502
CONVERTING A FLOATING POINT NUMBER TO AN 8-BIT NUMBER IN THE INTEGER FORMAT
1504
PLACING THE NUMBER IN THE INTEGER FORMAT IN A REGISTER OF A SECOND SET OF REGISTERS IN A PACKED FORMAT
1506
END

Fig. 15

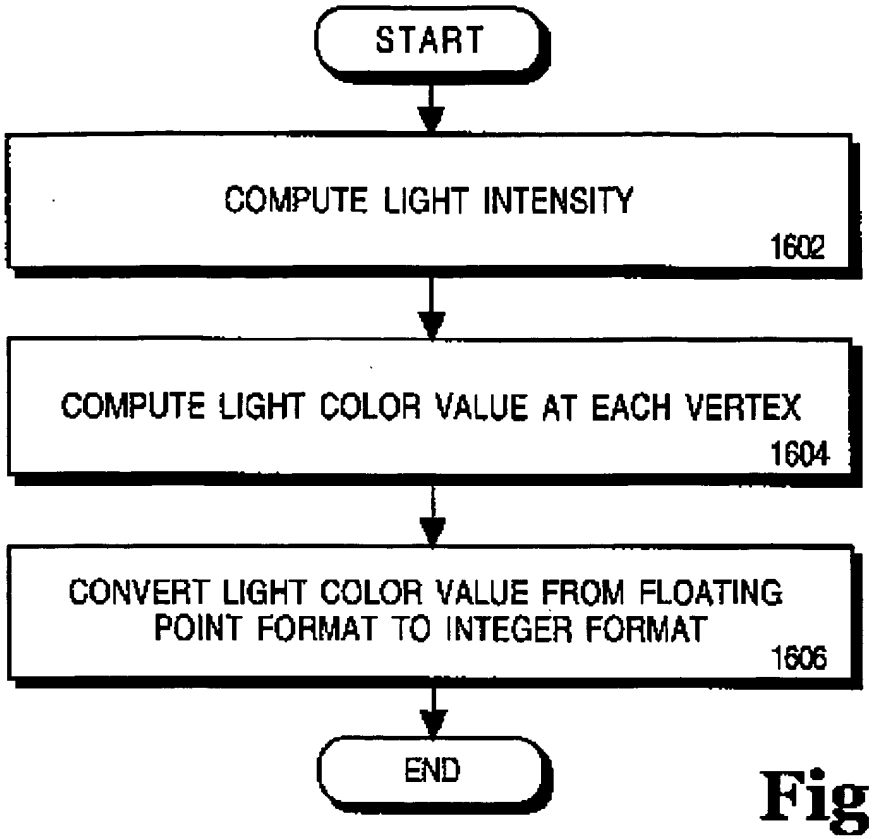

START
COMPUTE LIGHT INTENSITY
1602
COMPUTE LIGHT COLOR VALUE AT EACH VERTEX
1604
CONVERT LIGHT COLOR VALUE FROM FLOATING POINT FORMAT TO INTEGER FORMAT
1606
END

Fig. 16

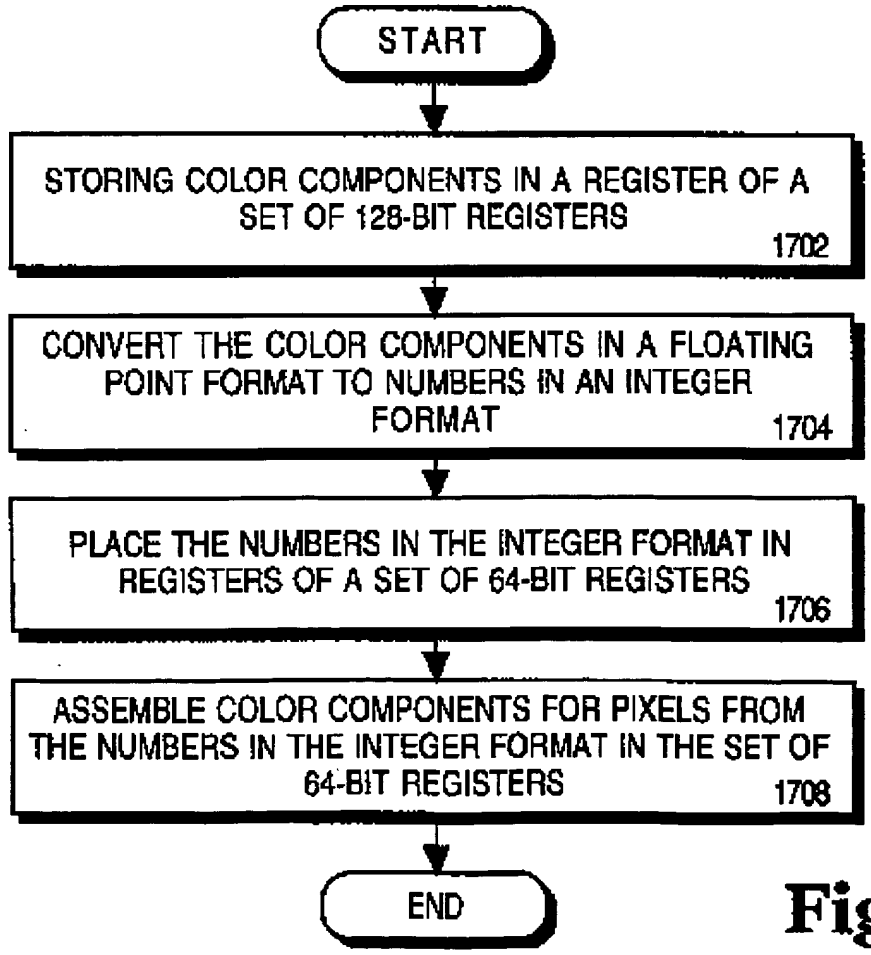

START
STORING COLOR COMPONENTS IN A REGISTER OF A SET OF 128-BIT REGISTERS
1702
CONVERT THE COLOR COMPONENTS IN A FLOATING POINT FORMAT TO NUMBERS IN AN INTEGER FORMAT
1704
PLACE THE NUMBERS IN THE INTEGER FORMAT IN REGISTERS OF A SET OF 64-BIT REGISTERS
1706
ASSEMBLE COLOR COMPONENTS FOR PIXELS FROM THE NUMBERS IN THE INTEGER FORMAT IN THE SET OF 64-BIT REGISTERS
1708
END

Fig. 17

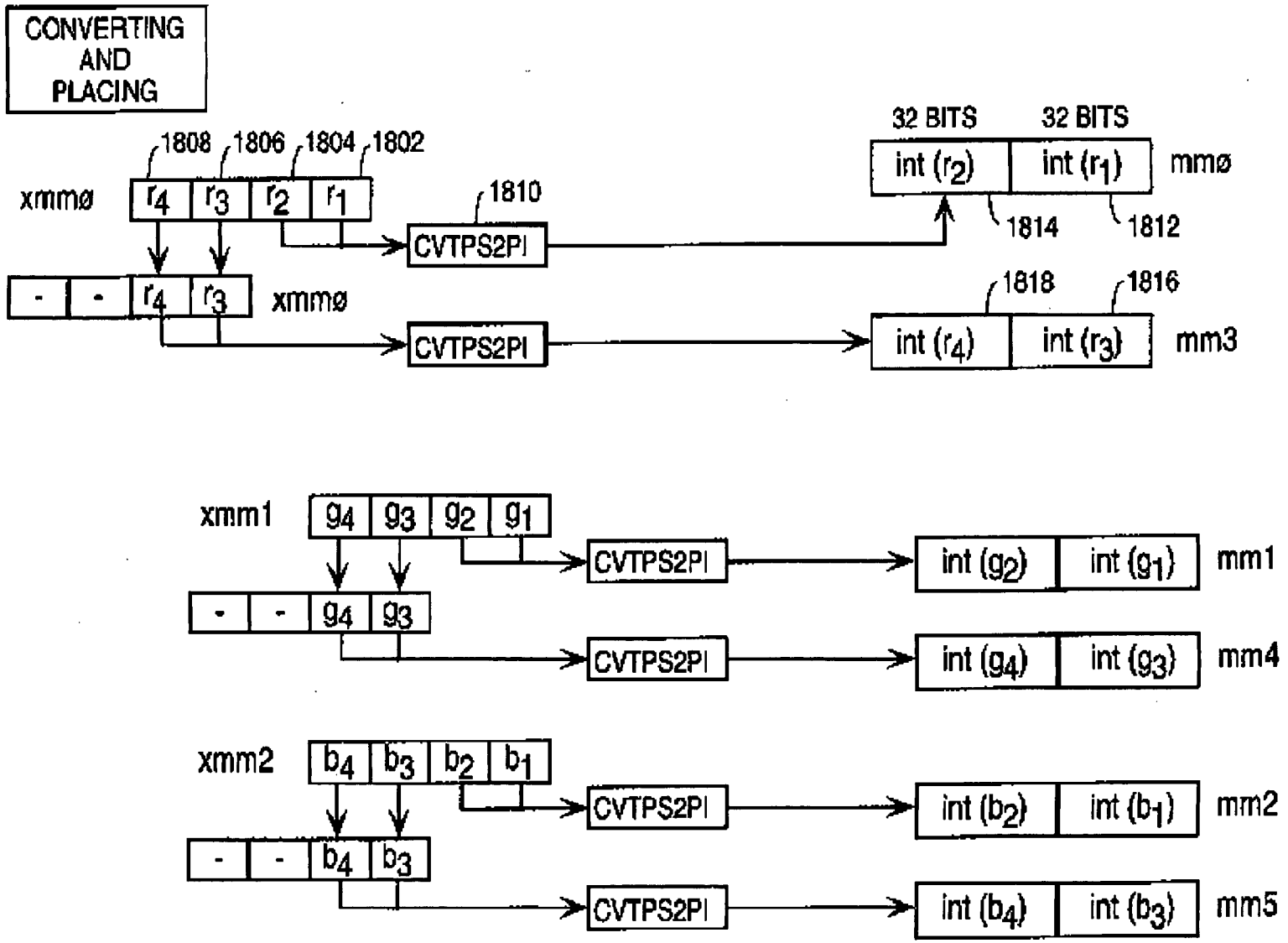

CONVERTING AND PLACING
xmmø
1808
1806
1804
1802
r4
r3
r2
r1
1810
CVTPS2PI
32 BITS
32 BITS
int (r2)
int (r1)
mmø
1814
1812
- - r4 r3
xmmø
CVTPS2PI
1818
1816
int (r4)
int (r3)
mm3
xmm1
g4 g3 g2 g1
CVTPS2PI
int (g2)
int (g1)
mm1
- - g4 g3
CVTPS2PI
int (g4)
int (g3)
mm4
xmm2
b4 b3 b2 b1
CVTPS2PI
int (b2)
int (b1)
mm2
- - b4 b3
CVTPS2PI
int (b4)
int (b3)
mm5

FIG. 18a

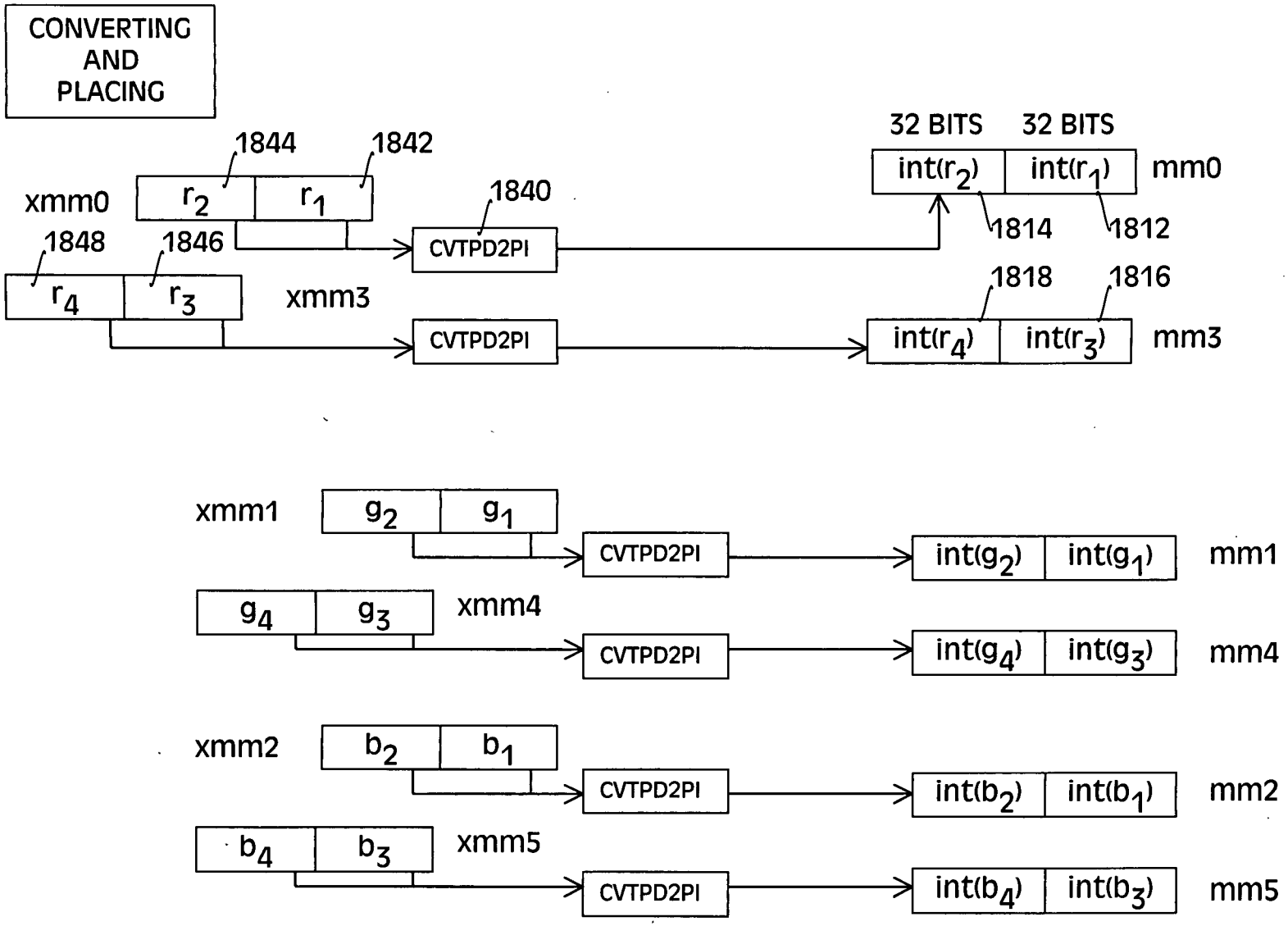

CONVERTING AND PLACING
32 BITS
32 BITS
1844
1842
xmm0
r2
r1
1840
int(r2)
int(r1)
mm0
1848
1846
1814
1812
r4
r3
xmm3
CVTPD2PI
1818
1816
int(r4)
int(r3)
mm3
xmm1
g2
g1
int(g2)
int(g1)
mm1
g4
g3
xmm4
int(g4)
int(g3)
mm4
xmm2
b2
b1
int(b2)
int(b1)
mm2
b4
b3
xmm5
int(b4)
int(b3)
mm5

FIG. 18b

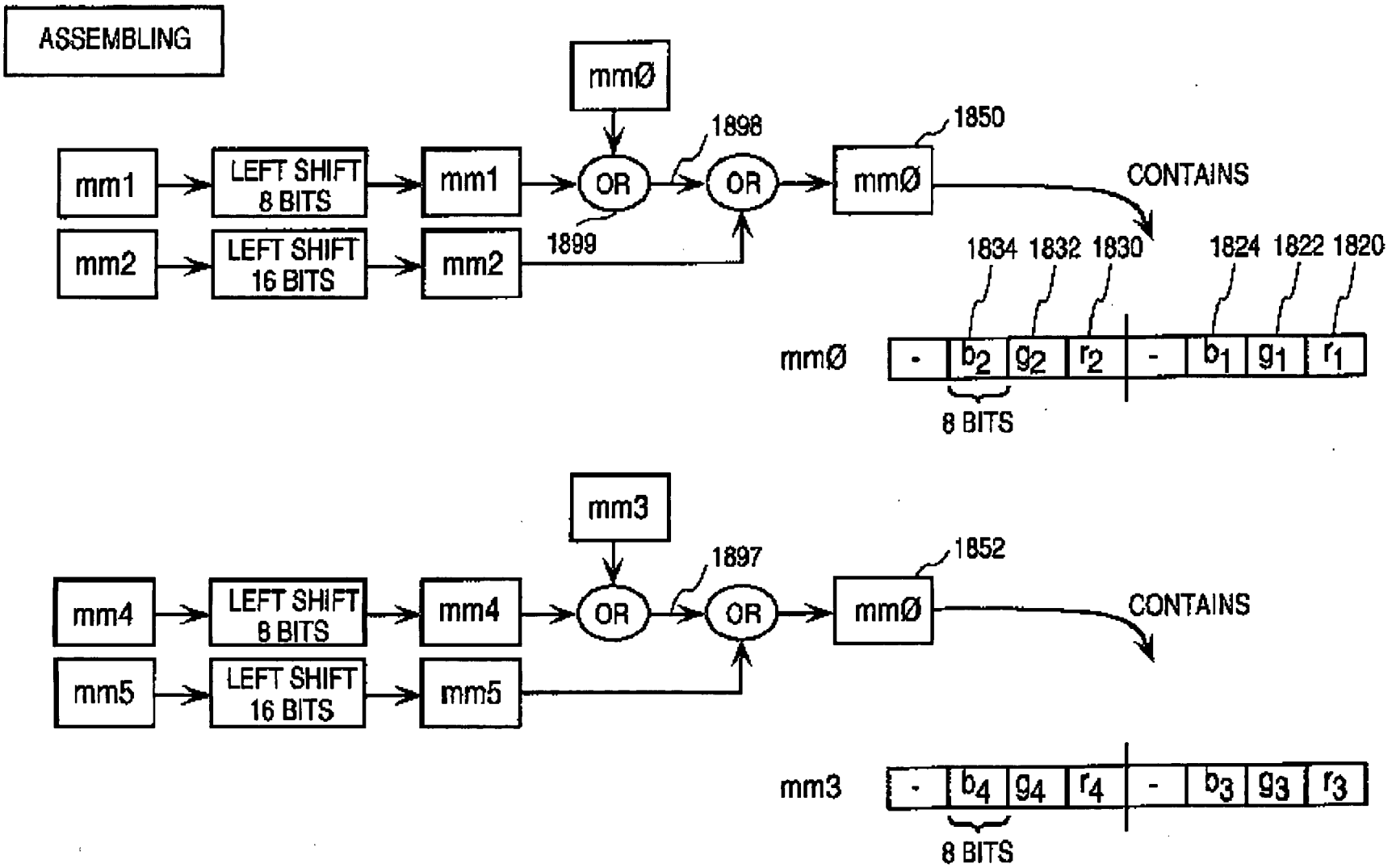

ASSEMBLING
mmØ
1898
1850
mm1
LEFT SHIFT 8 BITS
mm1
OR
OR
mmØ
CONTAINS
mm2
LEFT SHIFT 16 BITS
mm2
1899
1834 1832 1830
1824 1822 1820
mmØ
-
b2
g2
r2
-
b1
g1
r1
8 BITS
mm3
1897
1852
mm4
LEFT SHIFT 8 BITS
mm4
OR
OR
mmØ
CONTAINS
mm5
LEFT SHIFT 16 BITS
mm5
mm3
-
b4
g4
r4
-
b3
g3
r3
8 BITS

FIG. 18C

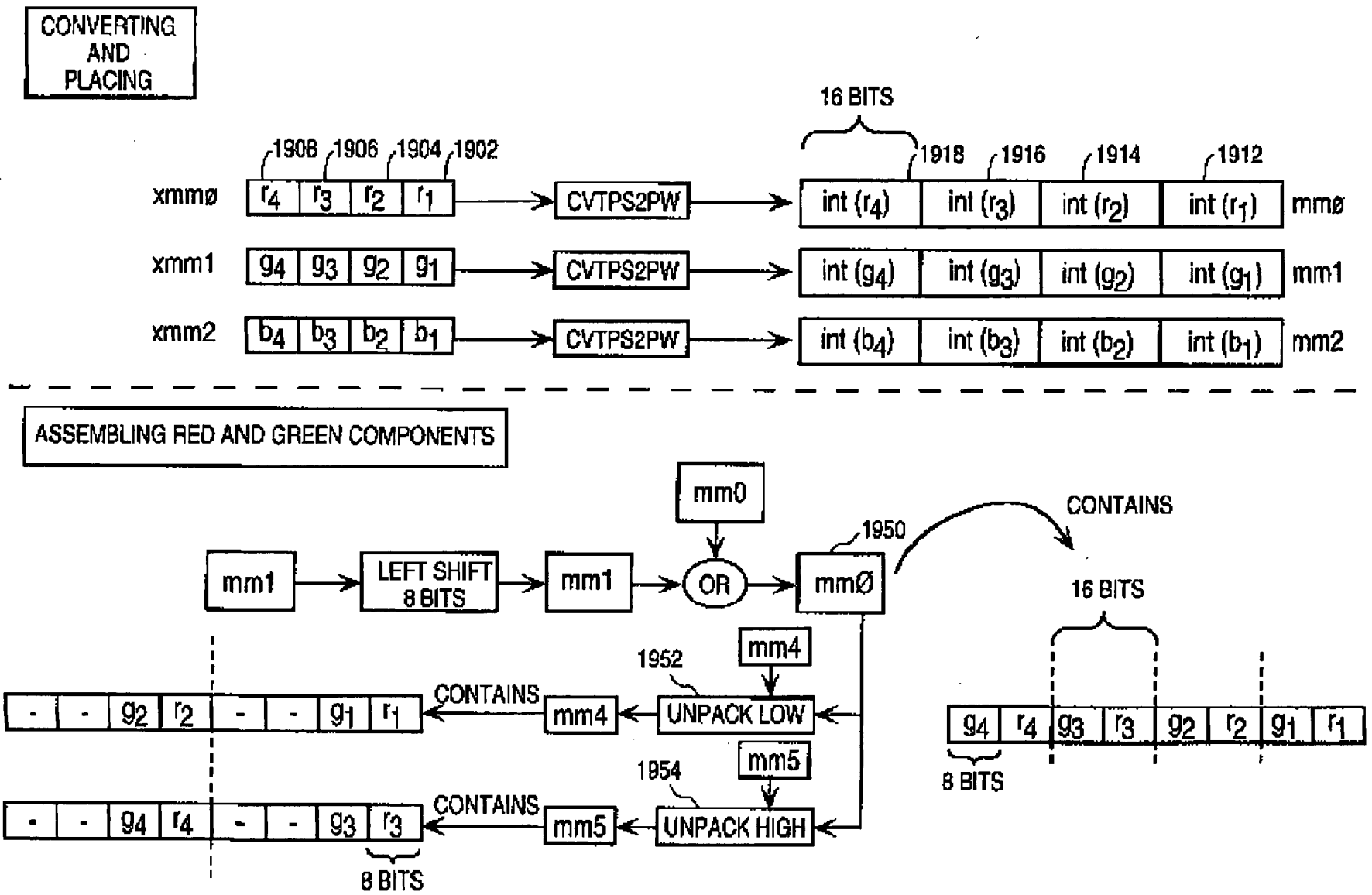

CONVERTING AND PLACING
16 BITS
1908
1906
1904
1902
1918
1916
1914
1912
xmmø
r4 r3 r2 r1
CVTPS2PW
int (r4) int (r3) int (r2) int (r1)
mmø
xmm1
g4 g3 g2 g1
CVTPS2PW
int (g4) int (g3) int (g2) int (g1)
mm1
xmm2
b4 b3 b2 b1
CVTPS2PW
int (b4) int (b3) int (b2) int (b1)
mm2
ASSEMBLING RED AND GREEN COMPONENTS
mm0
mm1
LEFT SHIFT 8 BITS
mm1
OR
mmØ
1950
CONTAINS
16 BITS
mm4
1952
- - g2 r2 - - g1 r1
CONTAINS
mm4
UNPACK LOW
g4 r4 g3 r3 g2 r2 g1 r1
8 BITS
mm5
1954
- - g4 r4 - - g3 r3
CONTAINS
mm5
UNPACK HIGH
8 BITS

Fig. 19a

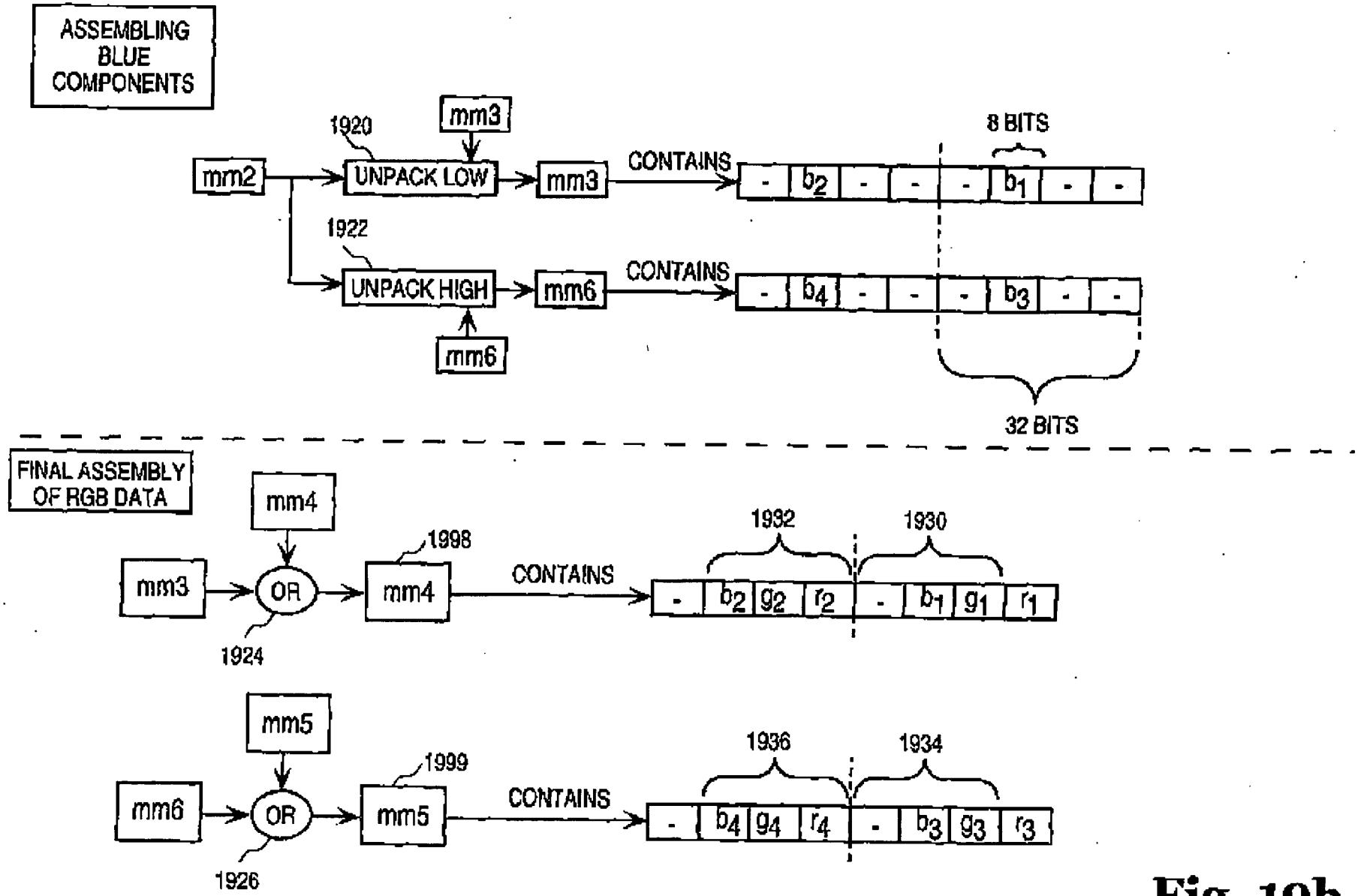

ASSEMBLING BLUE COMPONENTS
1920
mm3
8 BITS
mm2
UNPACK LOW
mm3
CONTAINS
- b2 - - - b1 - -
1922
UNPACK HIGH
mm6
CONTAINS
- b4 - - - b3 - -
mm6
32 BITS
FINAL ASSEMBLY OF RGB DATA
mm4
1998
1932
1930
mm3
OR
mm4
CONTAINS
- b2 g2 r2 - b1 g1 r1
1924
mm5
1999
1936
1934
mm6
OR
mm5
CONTAINS
- b4 g4 r4 - b3 g3 r3
1926

Fig. 19b

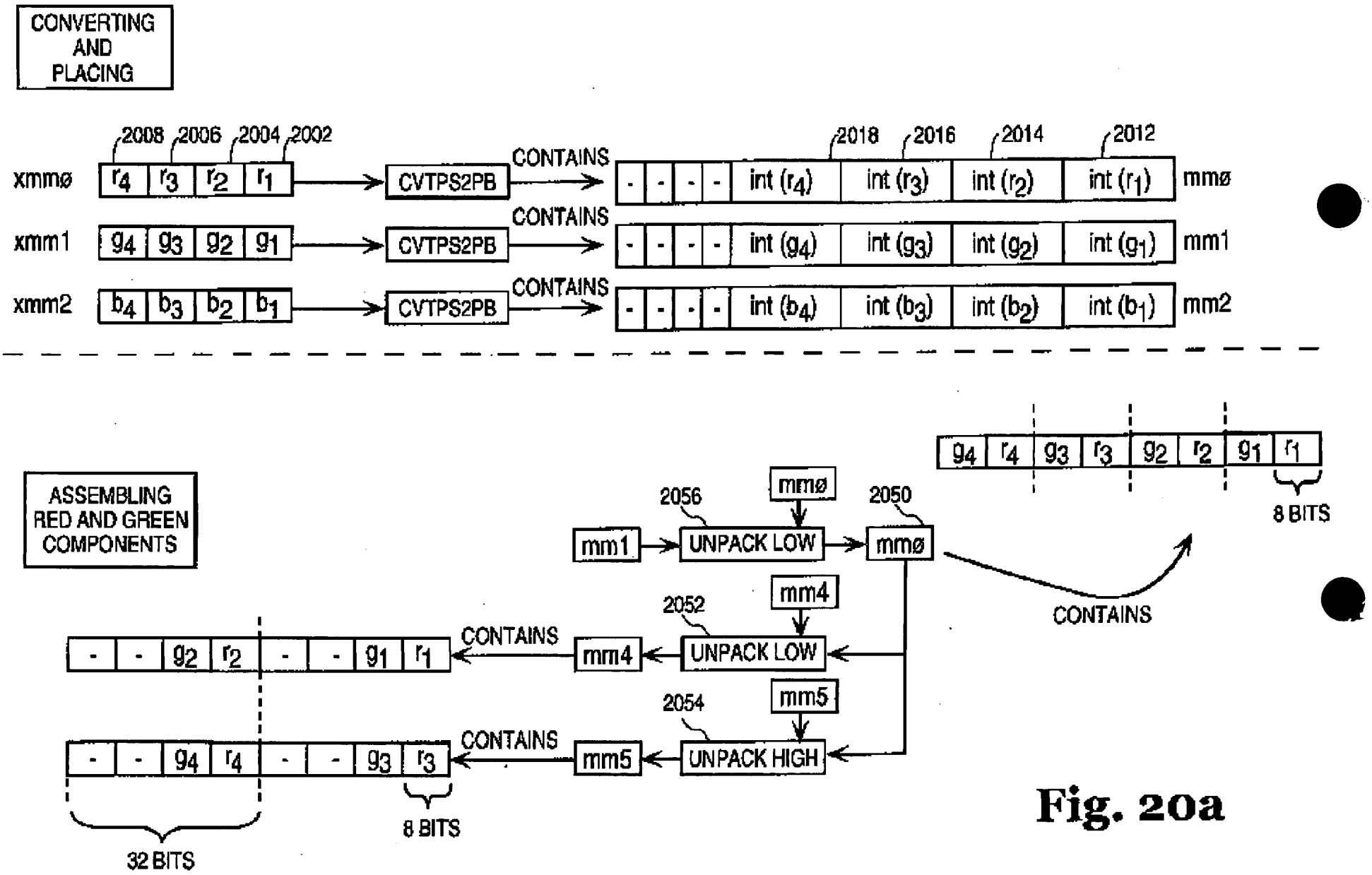

CONVERTING AND PLACING
2008
2006
2004
2002
xmmø
r4 r3 r2 r1
CVTPS2PB
CONTAINS
2018
2016
2014
2012
- - - - int (r4) int (r3) int (r2) int (r1)
mmø
xmm1
g4 g3 g2 g1
CVTPS2PB
CONTAINS
- - - - int (g4) int (g3) int (g2) int (g1)
mm1
xmm2
b4 b3 b2 b1
CVTPS2PB
CONTAINS
- - - - int (b4) int (b3) int (b2) int (b1)
mm2
ASSEMBLING RED AND GREEN COMPONENTS
mmø
2056
mm1
UNPACK LOW
2050
mmø
g4 r4 g3 r3 g2 r2 g1 r1
8 BITS
CONTAINS
mm4
2052
UNPACK LOW
mm4
CONTAINS
- - g2 r2 - - g1 r1
mm5
2054
UNPACK HIGH
mm5
CONTAINS
- - g4 r4 - - g3 r3
8 BITS
32 BITS

Fig. 20a

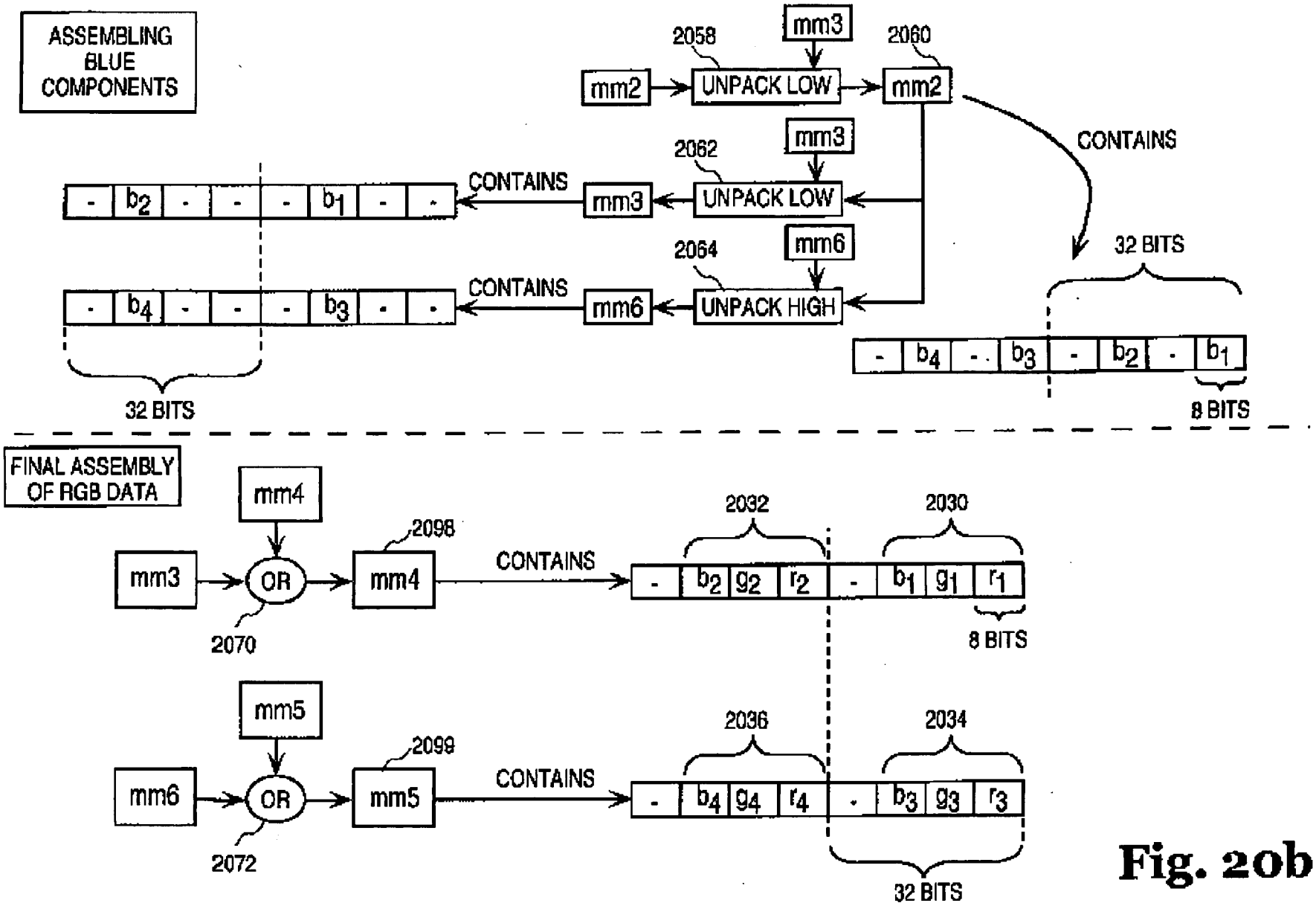

ASSEMBLING BLUE COMPONENTS
mm3
2058
2060
mm2
UNPACK LOW
mm2
CONTAINS
mm3
2062
UNPACK LOW
mm3
CONTAINS
mm6
2064
UNPACK HIGH
mm6
CONTAINS
32 BITS
32 BITS
8 BITS
FINAL ASSEMBLY OF RGB DATA
mm4
2098
mm3
OR
mm4
CONTAINS
2070
2032
2030
8 BITS
mm5
2099
mm6
OR
mm5
CONTAINS
2072
2036
2034
32 BITS

Fig. 20b

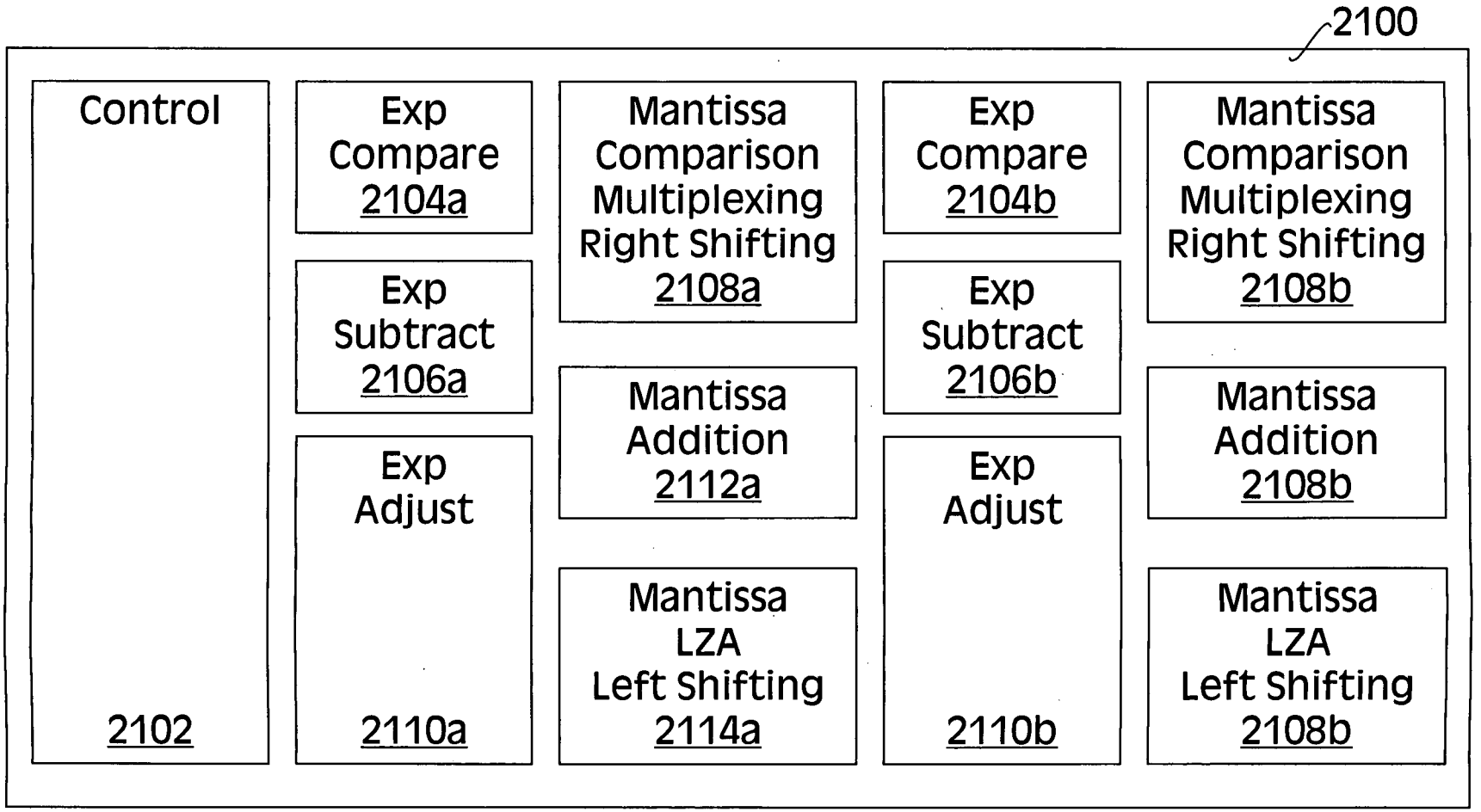


FIG. 21

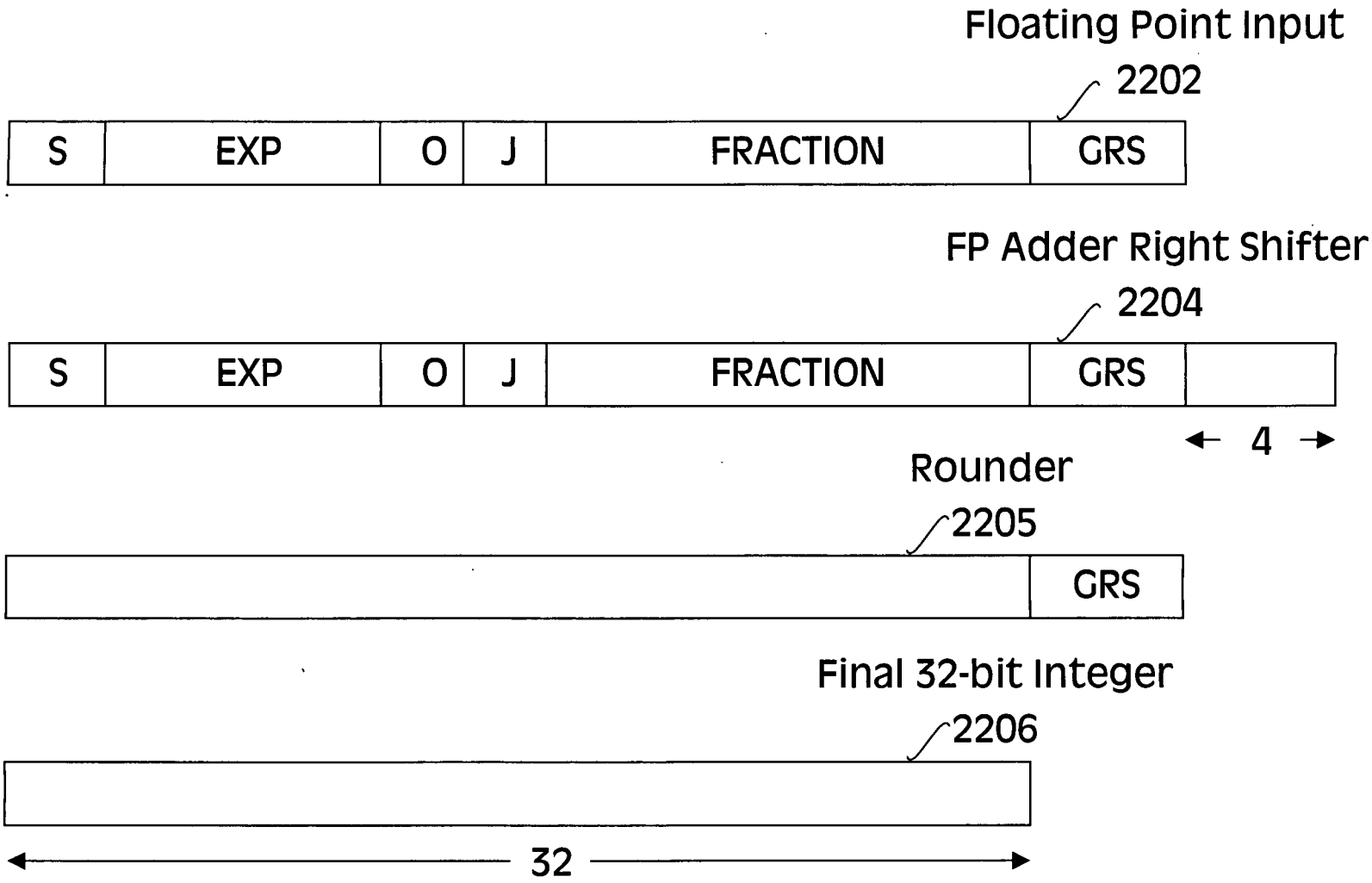


FIG. 22

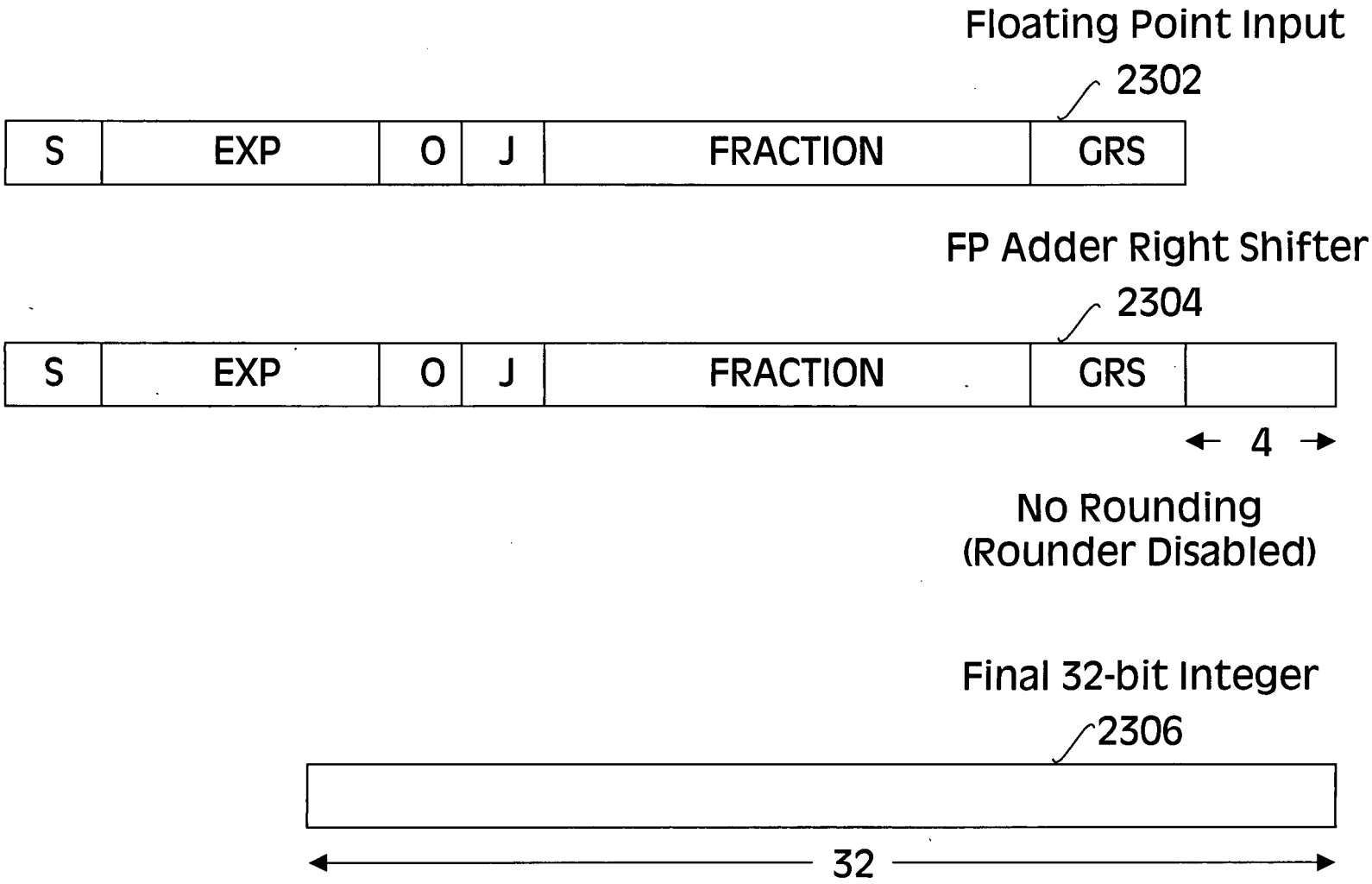


FIG. 23

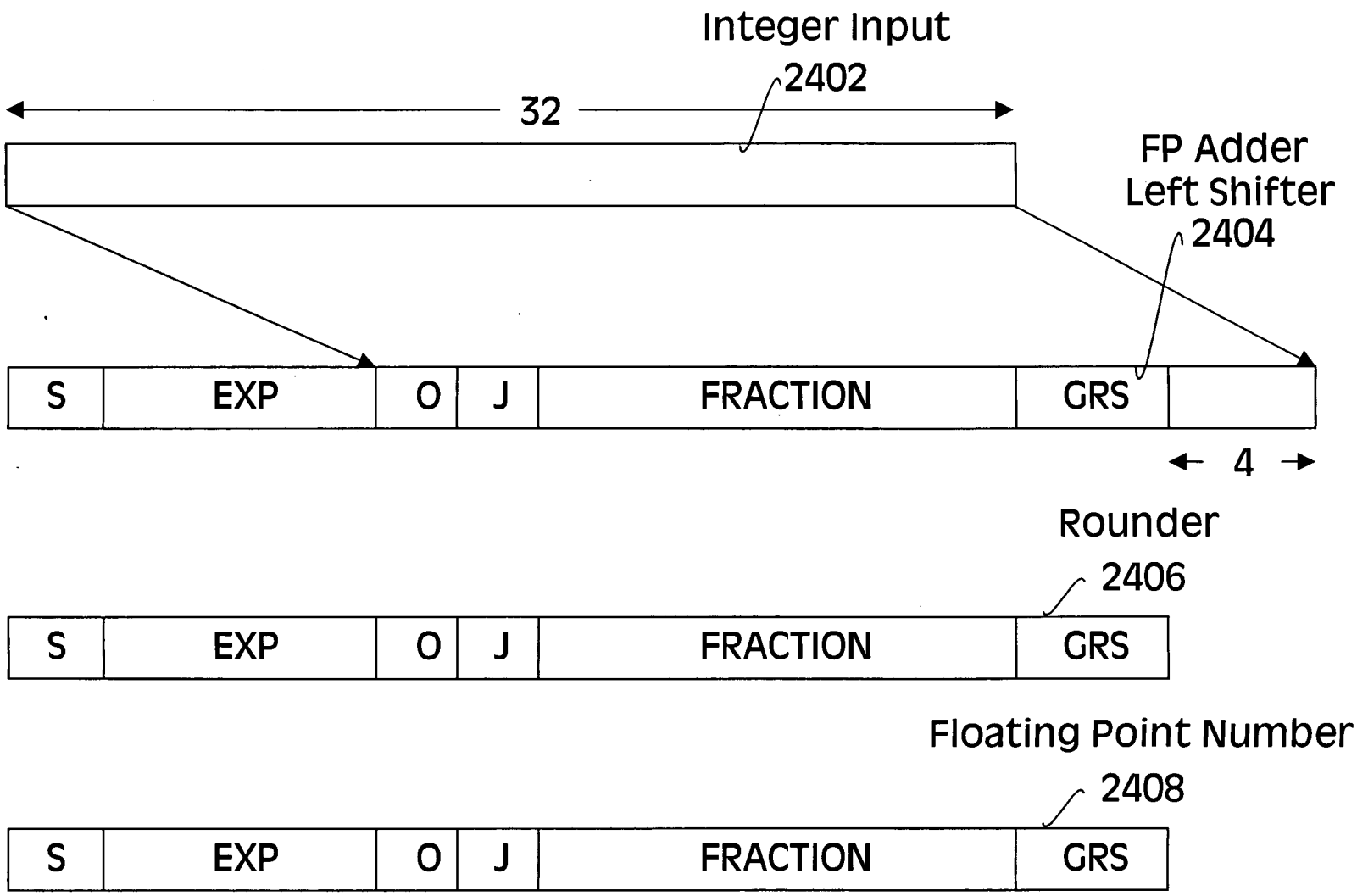


FIG. 24

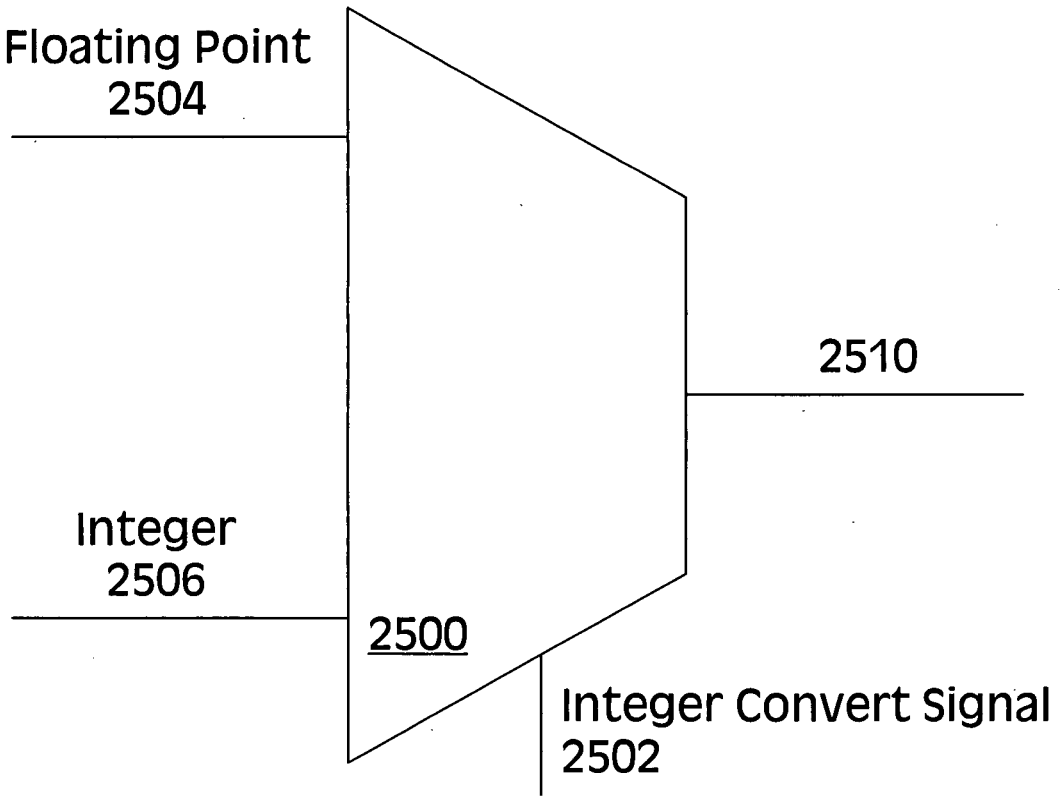


FIG. 25

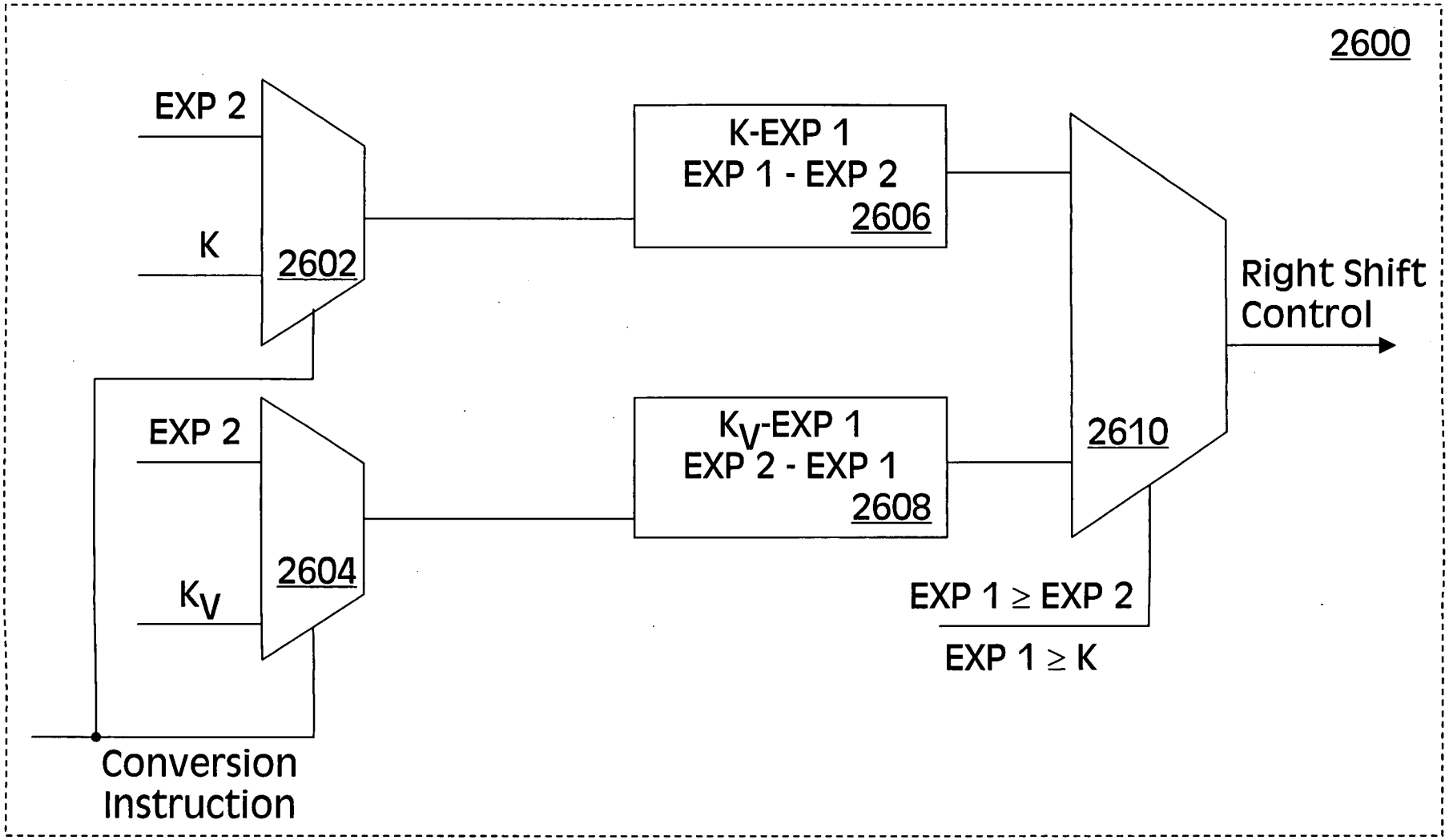

2600
EXP 2
K
2602
K-EXP 1
EXP 1 - EXP 2
2606
Right Shift
Control
EXP 2
K_V
2604
K_V-EXP 1
EXP 2 - EXP 1
2608
2610
EXP 1 ≥ EXP 2
EXP 1 ≥ K
Conversion
Instruction

FIG. 26